National Aeronautics and Space Administration
Jet Propulsion Laboratory
California Institute of Technology

HALT/HASS and Thermal Cycling to Assess COTS Boards, GoPro Camera and Advanced PBGA/CCGA *Virtex-5* Electronic Packages*

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Unclassified

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❖ To be presented by Rajeshuni Ramesham at the NEPP Electronics Technology Workshop (ETW). June 23-26, 2015 at NASA/GSFC in Greenbelt, MD

Outline

- Introduction
- Objectives
- Hardware to be assessed
  - COTS Xilinx and Microsemi ProASIC Boards
  - Advanced CCGA/*Virtex-5* Daisy Chain Package (Kyocera)
  - Assembled Advanced SMT packages (PBGA)
  - COTS GoPro Camera
- Experimental Details
- Test Results/Discussion
- Summary
- Acknowledgements

HALT Task Update

Task Plan

- **Functional Characterization of COTS boards:** Started functional tests, preliminary baseline results are provided vs., temperature (hot and cold temperature).
- **Willoughby Environmental Stress Screening**
  - Implementation of temperature variation during Willoughby Environmental Stress Screening (ESS) test using random vibration spectrum needs a hot and cold platform. Therefore, designed a hot and cold platform to cover a temperature range of -65°C to +125°C during Environmental Stress Screening (ESS) spectrum implementation with shaker table in ETQL labs.
  - Design of test article holder fixture is in the planning for various COTS boards.
  - **Completed test fixture design and fabrication for RV table.** Need to implement the test the fixture.
- **Highly Accelerated Life Testing (HALT)**
  - Data logging system is completed for HALT.
  - Began initial experiments with PBGA test boards in a temperature range of -65°C to +125°C. Tests will be started in the following order.
    - **Case 1:** Temperature Step Stress Test
    - **Case 2**: Rapid Thermal Transitions Stress Test
    - **Case 3**: Shock Step Stress Test at a constant temperature
    - **Case 4**: Combined Rapid Thermal Transitions Stress and Shock Test
- **CCGA 1752/*Virtex-5* daisy chain package to determine baseline thermal cycling test data.**
- **Thermal Cycling Assessment of GoPro Camera for NASA applications**
- **Analysis of Post HALT, HASS, Dynamic, and Thermal tests studies**
- **Verification of observations**
- **Prepare Reports/Final Report**

Hardware to be Assessed with HALT, HASS, Dynamic, and Thermal Cycling

- PBGA test board designed and manufactured. This board has been harnessed and the HALT test and thermal tests are in progress.
- COTS GoPRO Camera (candidate camera for Mars Helicopter project, Mars 2020)
- Evaluation Platform Xilinx ML507 FPGA Evaluation Board *Virtex-5* Xilinx
- Microsemi ProASIC3/E Evaluation FPGA Board
- Xilinx SPARTAN-6 FPGA SP601
- High I/O assembled CCGA packages *(Virtex-5 and other potential Packages)*

Introduction

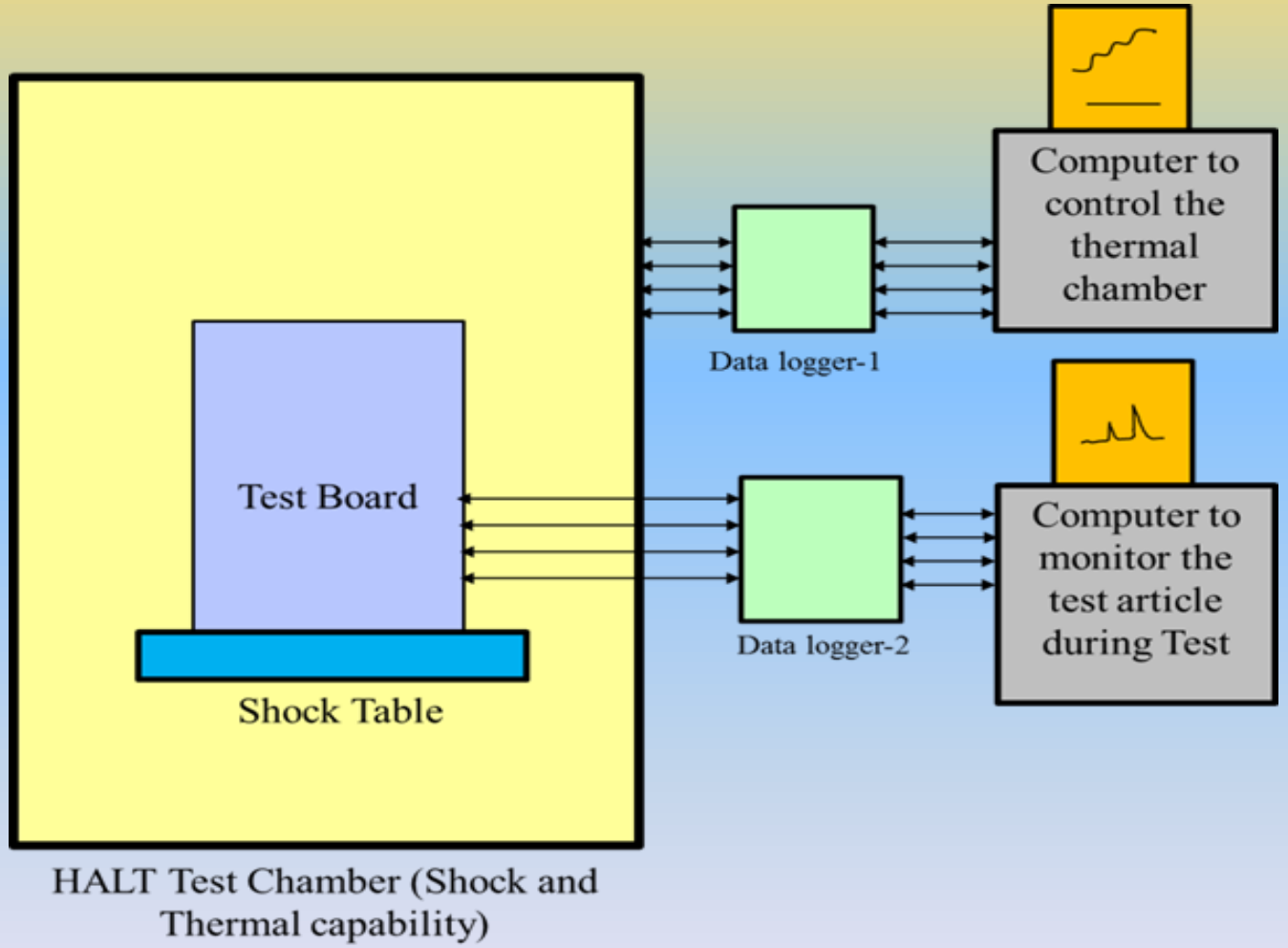
- Explore Highly Accelerated Life Testing (HALT), HASS, Thermal Cycling techniques to assess packaging designs and COTS boards, GoPRO camera design in a wide temperature range (–65°C to +125°C).
  - HALT is a custom hybrid package suite of testing technique, such as temperature down to -65°C to +125°C and vibration step processing up to 50g acceleration.
  - HALT testing implements repetitive multiple-axis vibration combined with thermal cycles testing of the test article to precipitate defects.
- HASS testing implements random vibration and thermal cycling testing of the test article to precipitate defects.
- Thermal cycling of the test article to precipitate defects performed over a long duration of thermal testing.
- Shock and Random vibration testing of the test article to precipitate defects in short test duration.

Objective

- Predict reliability, assess failure mechanism and assess survivability of selected advanced electronic interconnect packages (Plastic Ball Grid Arrays, Flip-chips, surface mount package interconnects, CCGA, GoPRO camera, etc.) for especially long duration missions in a shorter duration.
- Reduce the development cycle time for improvements to the packaging designs.

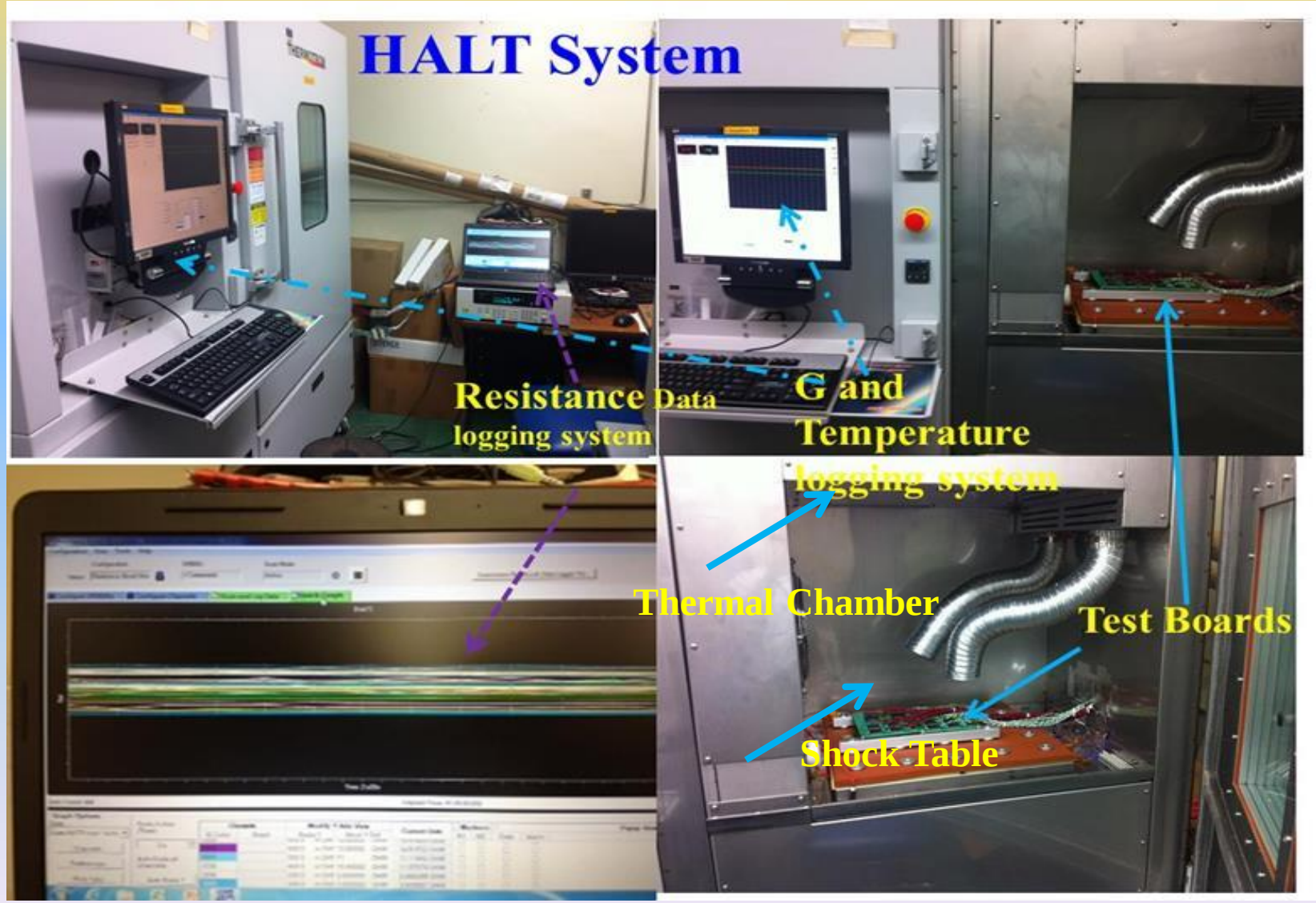
Experimental Details

- Design and build advanced test boards that are considered useful for a variety of NASA projects.
- Tested COTS Boards.
- Tested *Virtex-5* CCGA boards
- Assessed COTS GoPRO camera.
- Select stress stimuli thermal cycling and/or all-axis vibration or both simultaneously
- Perform stress testing
- Analyze the test results and compare with the thermal cycling test data.
- Estimate the acceleration factor for package failures observed.



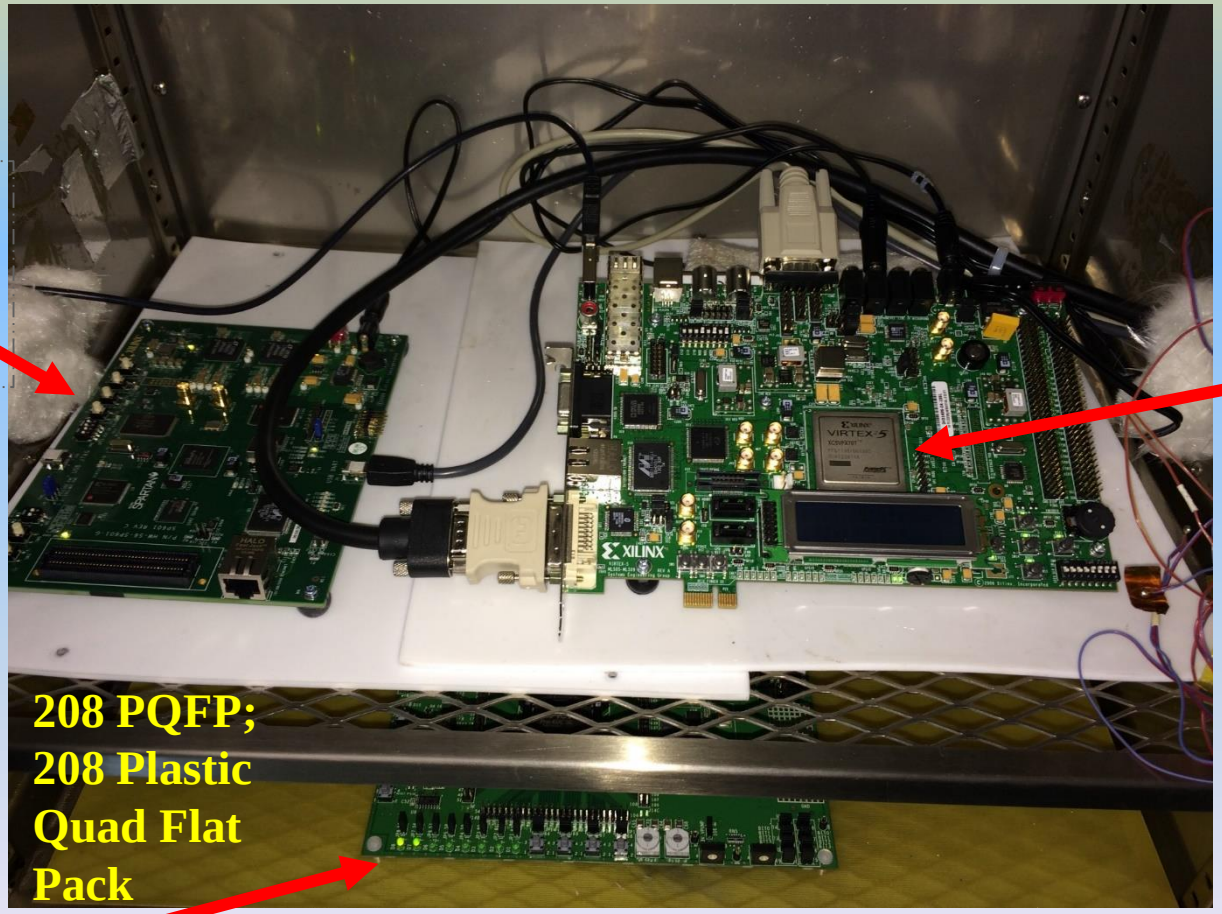
Schematic diagram for the solder joint continuity monitoring HALT test system

Test Boards in the HALT System



COTS Test Boards

COTS Evaluation Boards in the Thermal Chamber (Obtained Baseline Test Data vs. Temperature)



SPARTAN-6 FPGA SP601 EVALUATION Board

256 Fine-Pitch Ball Grid Arrays

Virtex-5 FPGA ML50X Family Board (Front)

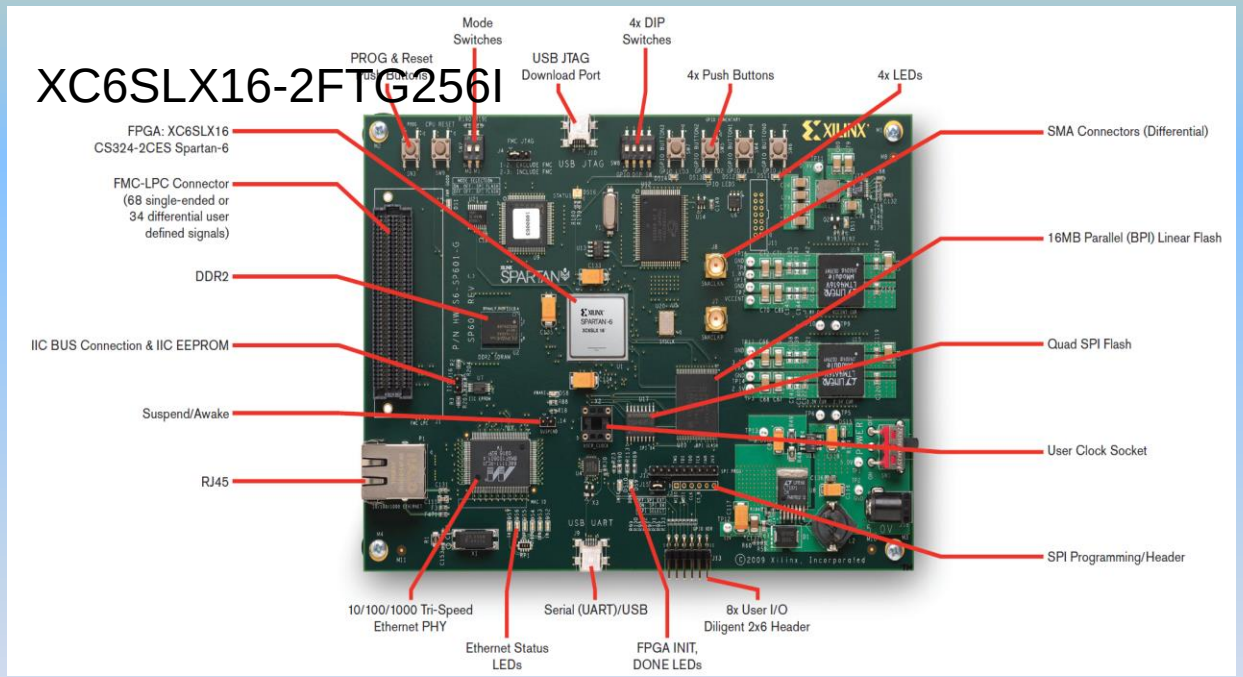
1136 FCBGA: 1136 Flip Chip Ball grid Arrays

208 PQFP; 208 Plastic Quad Flat Pack

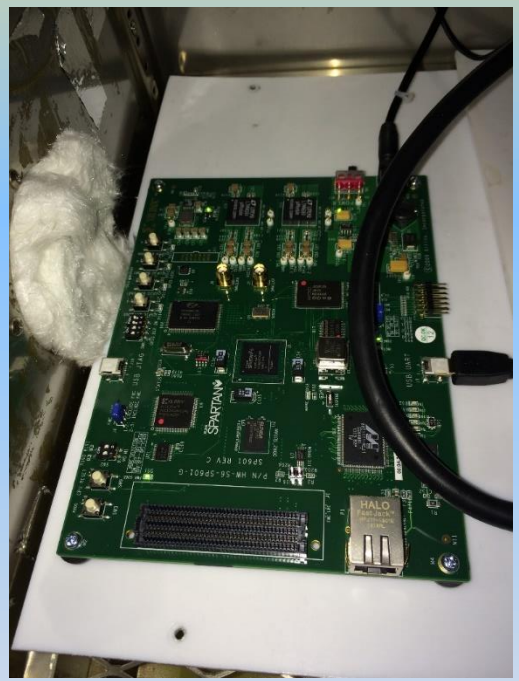
Micro semi ProASIC3/E Evaluation FPGA Board

SPARTAN-6 FPGA SP601 EVALUATION Board

256 FTBGA: 256 Fine-Pitch Ball Grid Arrays



Source: *http://www.xilinx.com/publications/prod_mktg/sp601_product_brief.pdf*

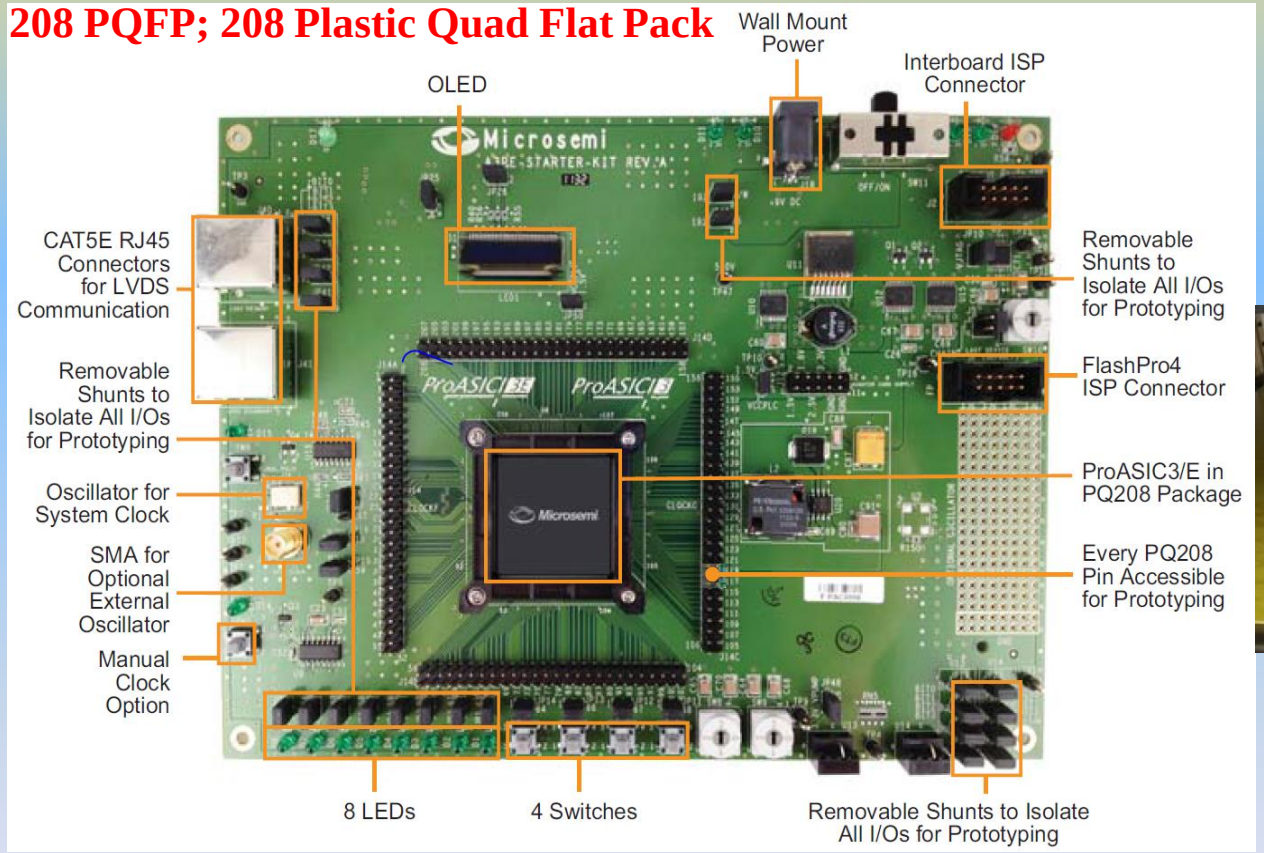


Board mounted in the thermal Chamber During the Tests

Xilinx SP601 FPGA Board-1 (Preliminary Thermal Test Results Summary)

	Xilinx SP601 FPGA Board-1 (Preliminary)											
		Tested ------>										
		Temperature, C										Remarks
Test #	**Test Performed to Health/Functional Check**	**+25**	**+50**	**+75**	**+100**	**+125**	**+25**	**0**	**-30**	**-30±10**	**-65**	**-60±10**	
1	Universal Asynchronous Receiver/Transmitter (UART)	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
2	Light Emitting Diodes	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS	PASS	Functional
3	Timer Test	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
4	Flash Memory	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
5	Inter-Integrated Circuit (IIC) Electrically Erasable Programmable Read-Only Memory (EEPROM)	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
6	ETHERNET Lite Test	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
7	General Purpose Input/output (GPIO) Switches	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
8	Multi-Port Memory Controller (MPMC) Memory Test or External Memory Test	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS		PASS	PASS		MPMC test failed @125C and recovered when the temperature reduced..

Micro semi ProASIC3/E Evaluation FPGA Board



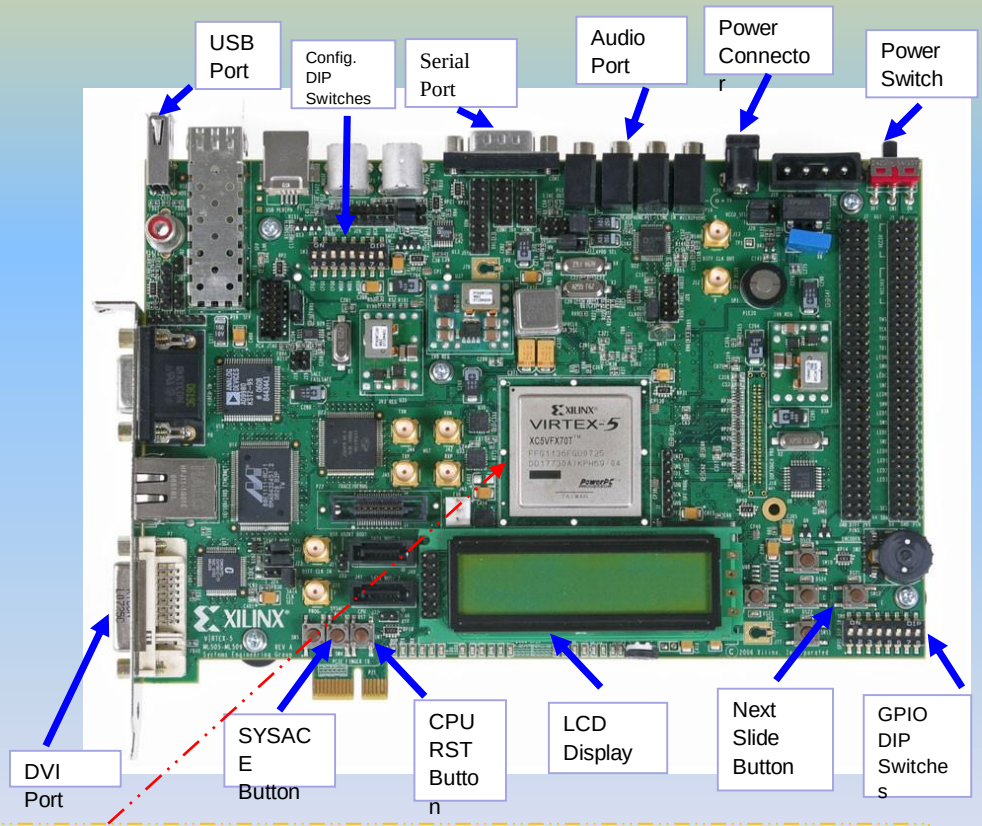
http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/proasic3/proasic3-starter-kit

Board mounted in the thermal Chamber During the Tests

Microsemi ProASIC3/E Evaluation FPGA Board (Preliminary Test Results Summary)

	Microsemi ProASIC3/E Evaluation Board-1 (Preliminary)											
		Tested ------>										
		Temperature, C										Remarks
Test #	**Test Performed to Health/Functional Check**	**+25**	**+50**	**+75**	**+100**	**+125**	**+25**	**0**	**-30**	**-30 ± 10**	**-65±10**	**-75±10**	
1	Flashing Light Emitting Diodes (LEDs) Demo: Right to Left	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
2	Flashing Light Emitting Diodes (LEDs) Demo: Left to Right	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	Functional
3	8-Bit Counter -- Count Up	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
4	8-Bit Counter -- Counting Down	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional
5	8-Bit Counter -- Counting Up or Down with Forced State	PASS	PASS	PASS	PASS	PASS	PASS	PASS		PASS		PASS	Functional

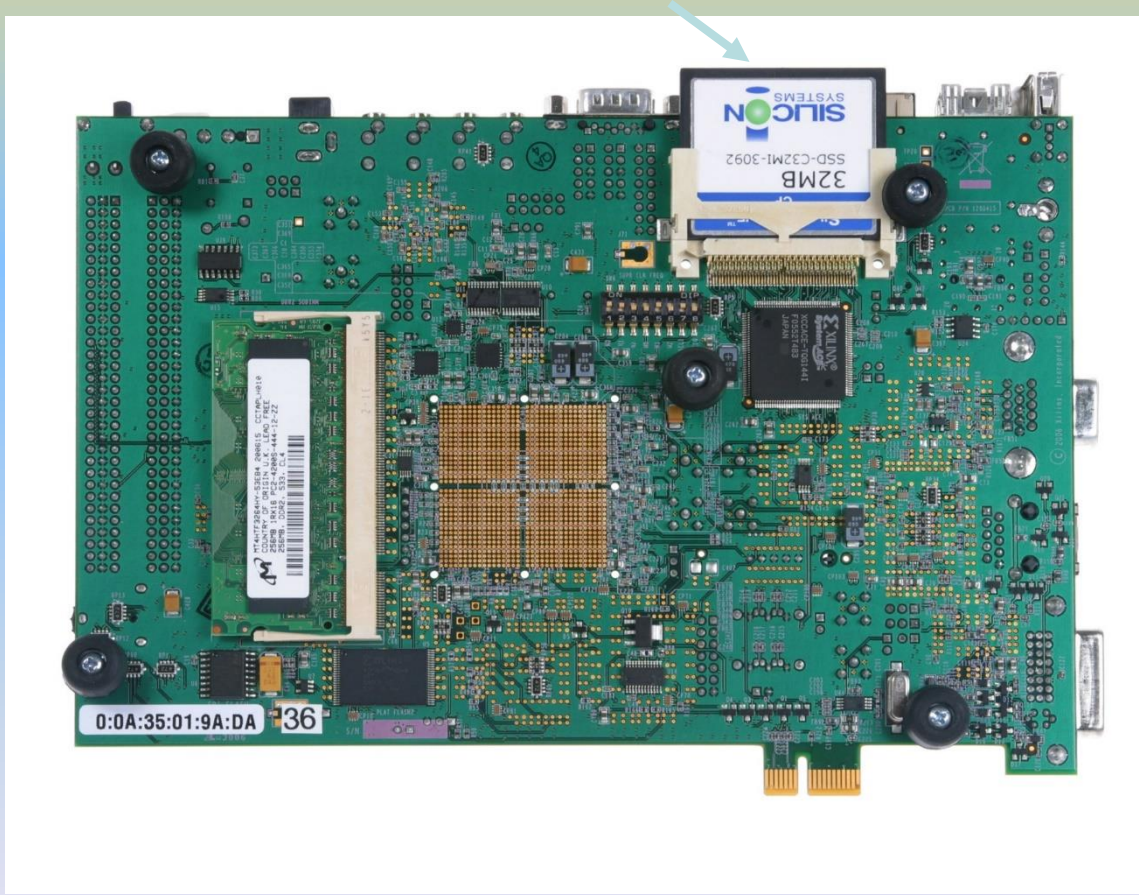
Detailed Description of Virtex-5 FPGA ML50X Family Components (Front)



1136 FCBGA: 1136 Flip Chip Ball grid Arrays

Board mounted in the thermal Chamber During the Tests

Detailed Description of Virtex-5 FPGA ML50X Family Components (Back)ML50x Evaluation Platform with CF Card



Source: http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf

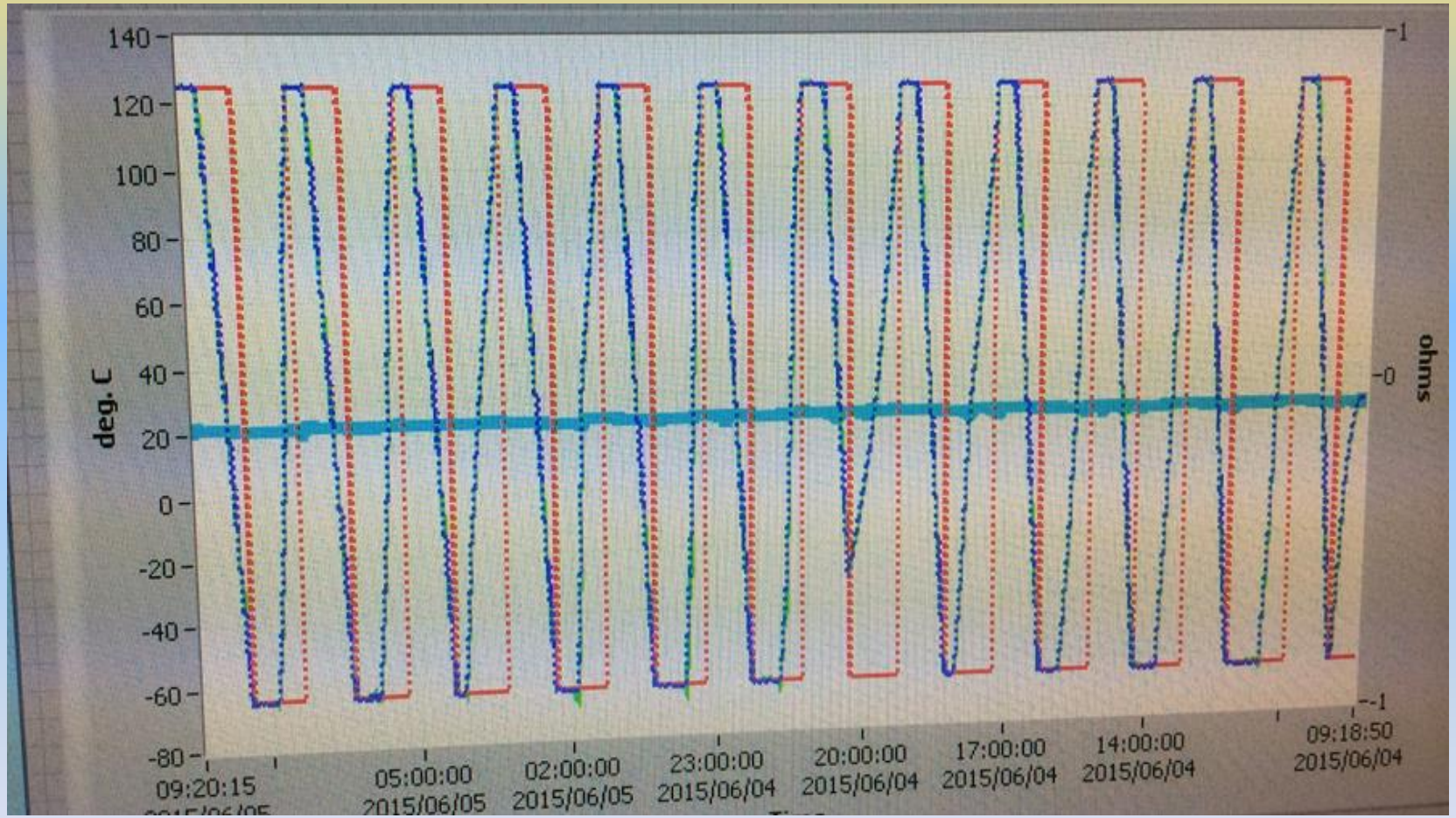
Xilinx ML507 FPGA Evaluation Board (Preliminary Test Results)

	Xilinx ML507 FPGA Evaluation Board (Preliminary)											
		Tested ------>										
		Temperature, C										Remarks
Test #	**Test Performed to Health/Functional Check**	**+25**	**+50**	**+75**	**+100**	**+125**	**+25**	**0**	**-30**	**-30±10**	**-65**	**-55±10**	
1	Virtex-5 Slide Show	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS		PASS		PASS	Recovered
2	Test Universal Serial Bus (USB) Demo	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS		PASS		PASS	Recovered
3	Test Doulbe Data Rate (DDR) Random Access Memory (RAM)	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS	PASS		PASS		Recovered
4	Test Zero Bust Turnaround (ZBT) Static Random-Access Memory (SRAM)	PASS	PASS	PASS	PASS	**FAIL, LEDs Went Black or Board is Black**	PASS	PASS	PASS		PASS		Recovered
5	Light Emirtting Diodes	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS	PASS	PASS	PASS		Recovered
6	Test Push Buttons	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS		PASS		PASS	Recovered
7	Test Dual in-line package (DIP) Switches	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS	PASS		PASS		Recovered
8	Test Character Liquid Crystal Display (LCD)	PASS	PASS	**FAIL (Hard to Read)**	**FAIL (Gray)**	**FAIL**	**FAIL, Characters Missing**	**No Visible FAIL**	**No Visible FAIL**	**No Visible FAIL**		**No Visible FAIL**	LCD did not recover fully. Characters missing.
9	Test Video Graphics Array (VGA) Output	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS	PASS		PASS		Recovered
10	Test Piezo Transducer	PASS	PASS	PASS	PASS	**FAIL**	PASS	PASS	PASS		PASS		Recovered

COTS FPGA Boards at -65ºC

Thermal Cycling of COTS Boards

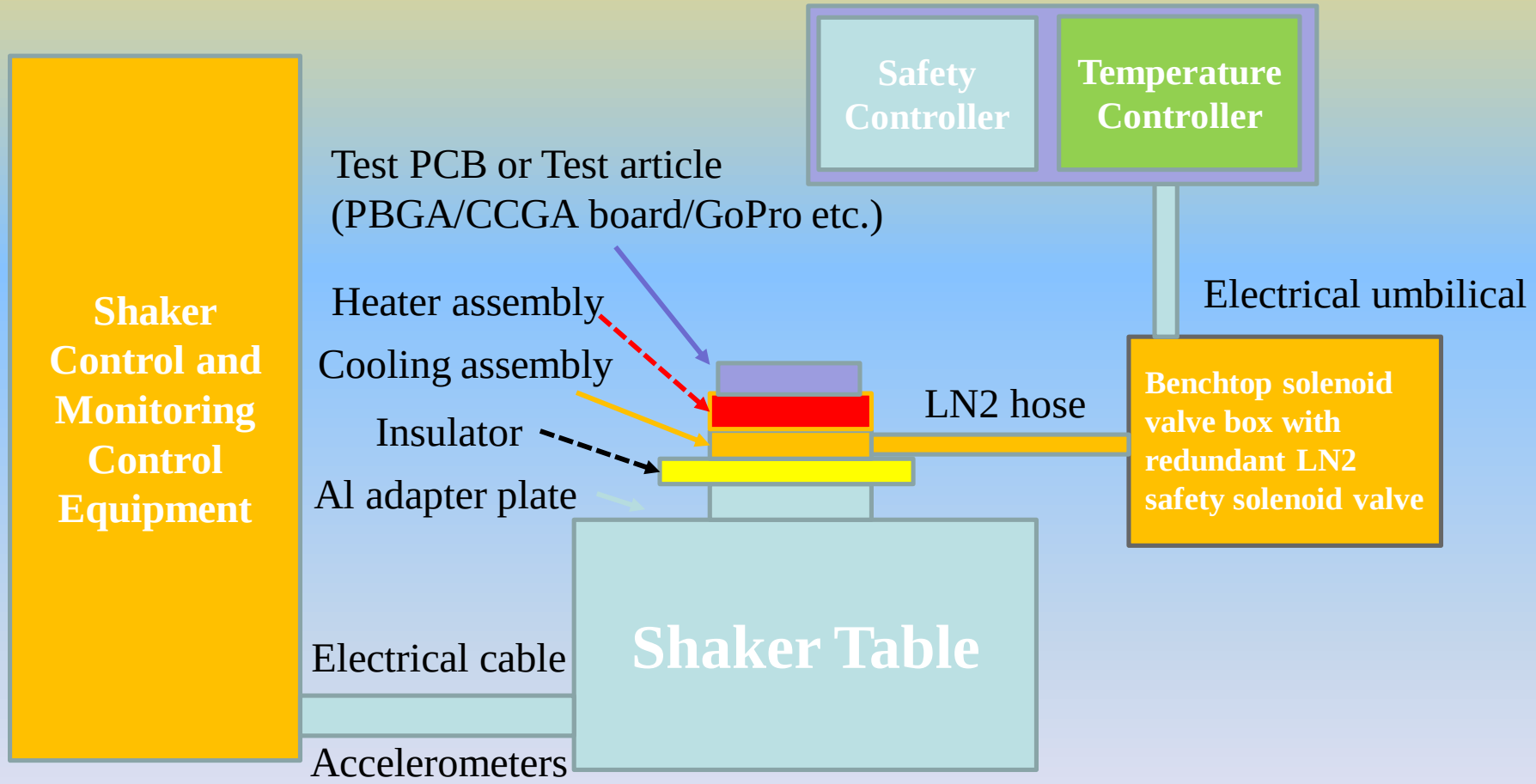
Temperature, C



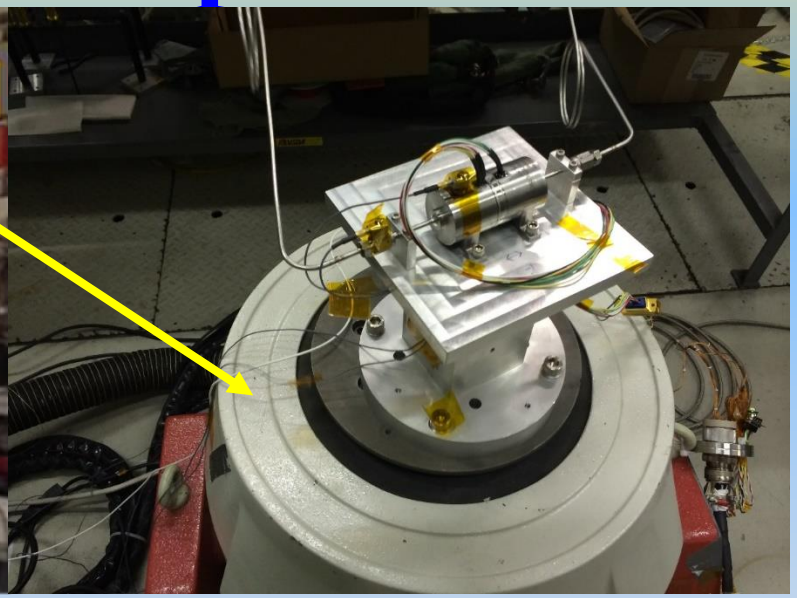
Time

Environmental Stress Screening (ESS)

Schematics of Willoughby Environmental Stress Screening (ESS) testing: -55ºC to +125ºC



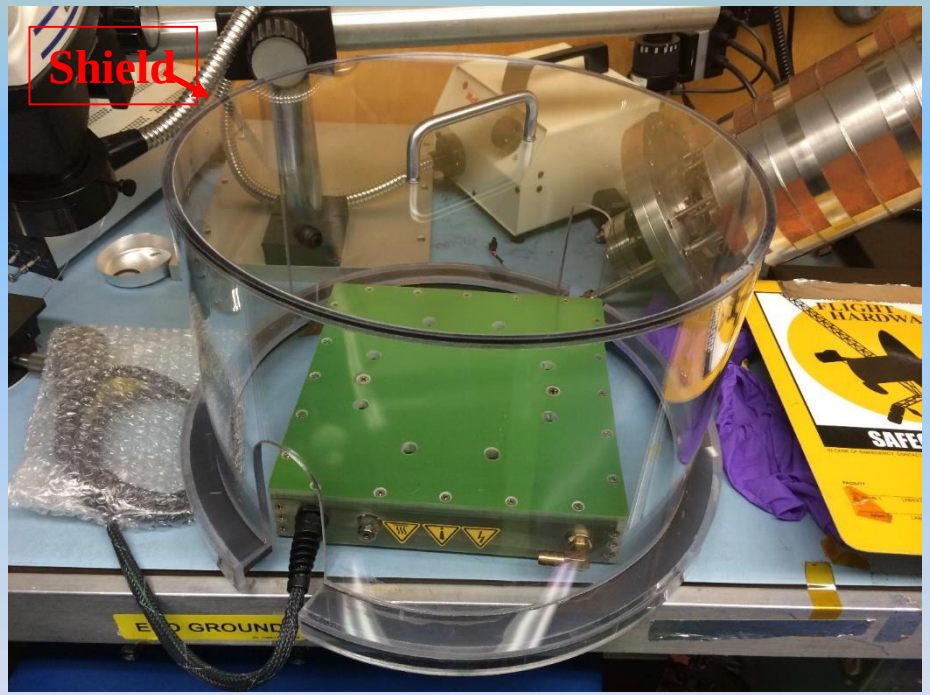
Shaker table to implement Willoughby ESS spectrum

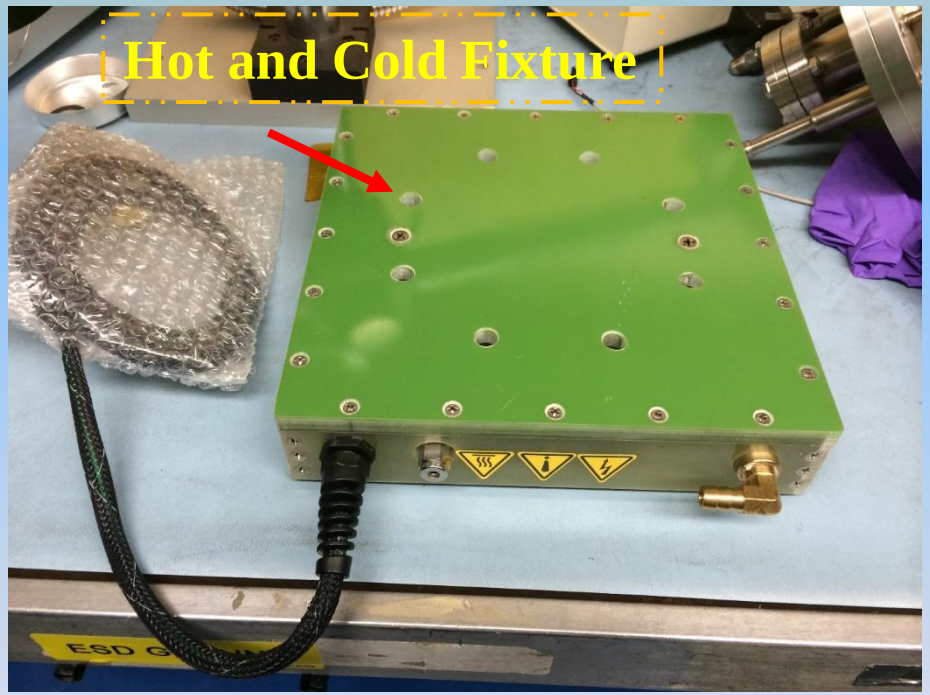


Shaker Table

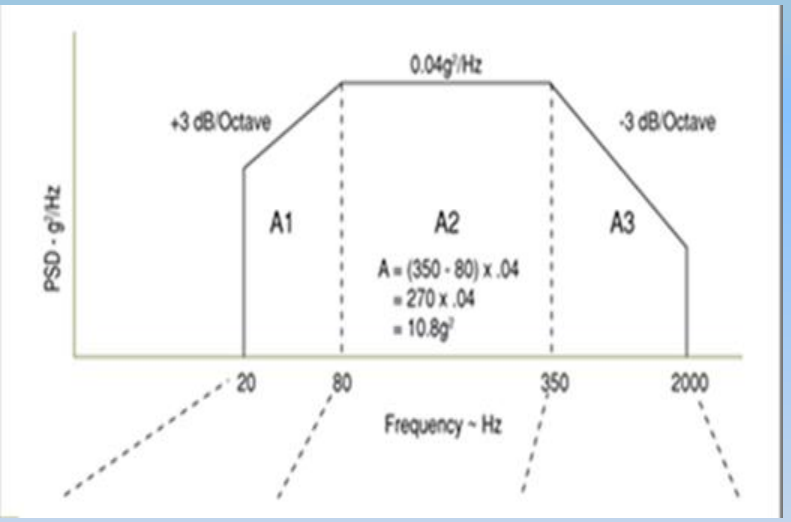
- Designed and Manufactured the hot-cold plate for -65°C to +125°C during ESS spectrum implementation with shaker table

Hot and Cold fixture for the RV Shaker Table





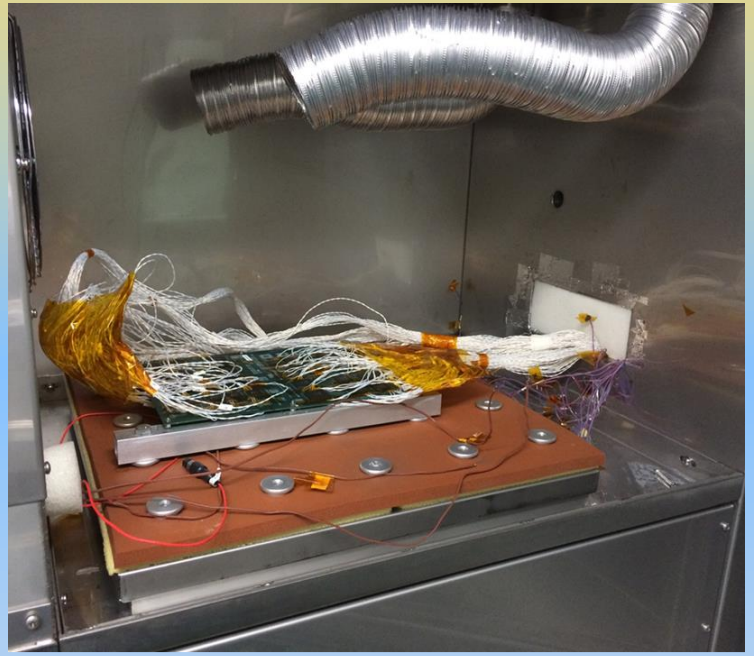
Willoughby ESS spectrum to test COTS Test Boards



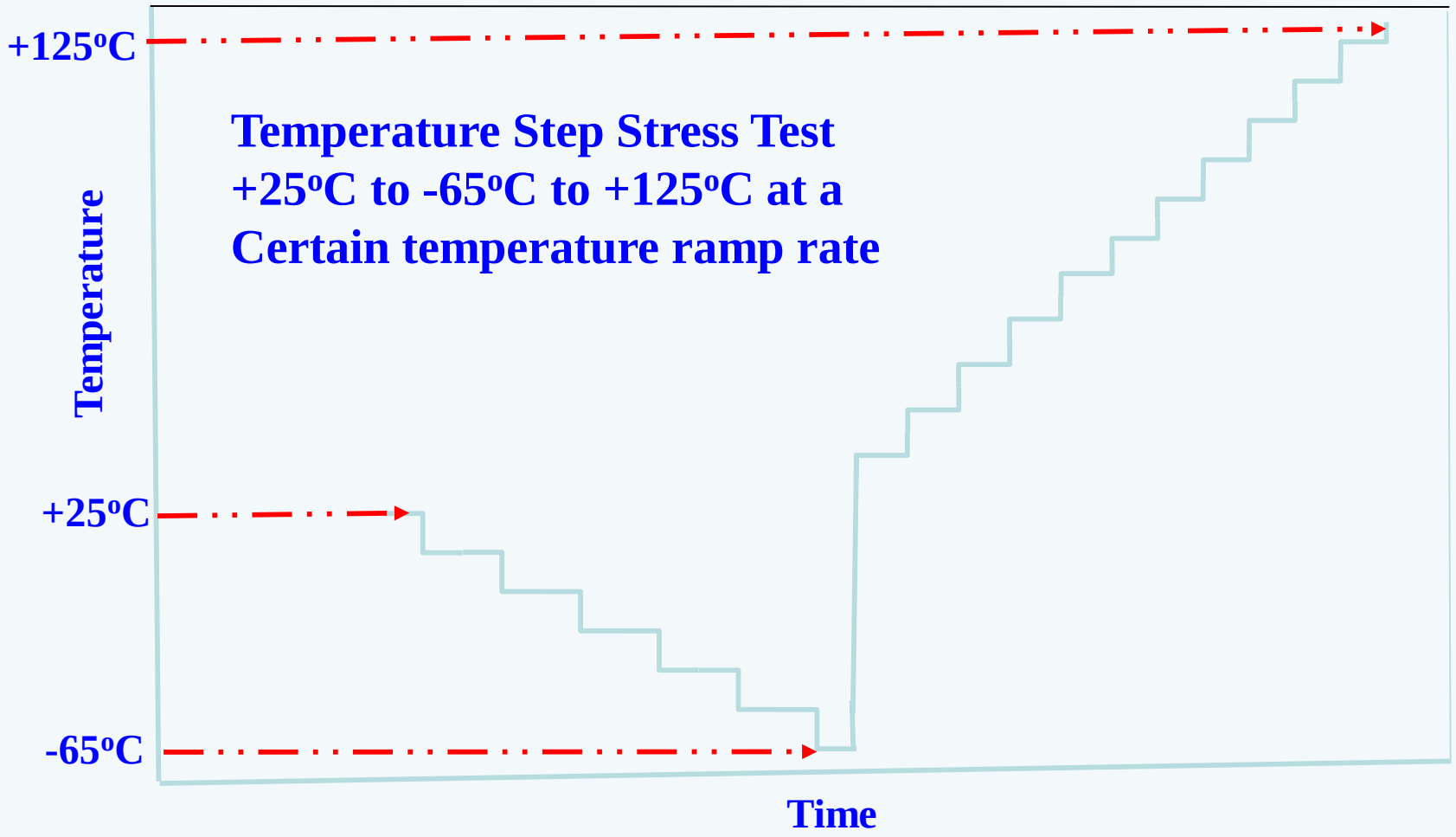
				Slope		Acceleration
FREQ(Hz)	ASD(G^2/Hz)	dB	OCT	dB/OCT	AREA	Grms
20.00	0.0100	*	*	*	*	*
80.00	0.0400	6.02	2.00	3.01	1.50	1.22
350.00	0.0400	0.00	2.13	0.00	12.30	3.51
2000.00	0.0070	-7.57	2.51	-3.01	36.70	**6.06**

- Random vibration test equipment to cover this acceleration range to implement the ESS spectrum is available for this effort
- Temperature variation capability during implementation of Willoughby ESS testing using above random vibration spectrum is in progress.

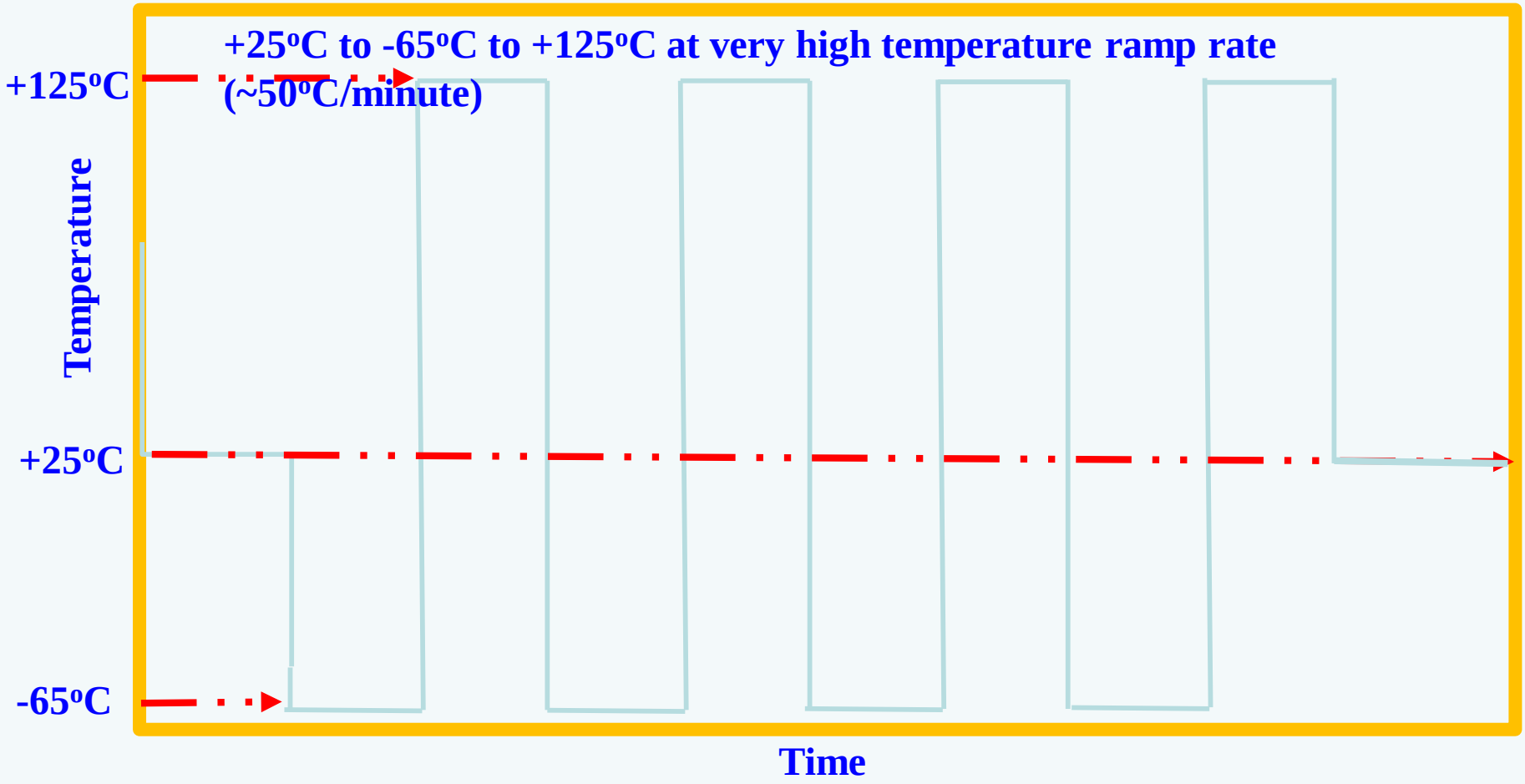
Highly Accelerated Life Testing (HALT)

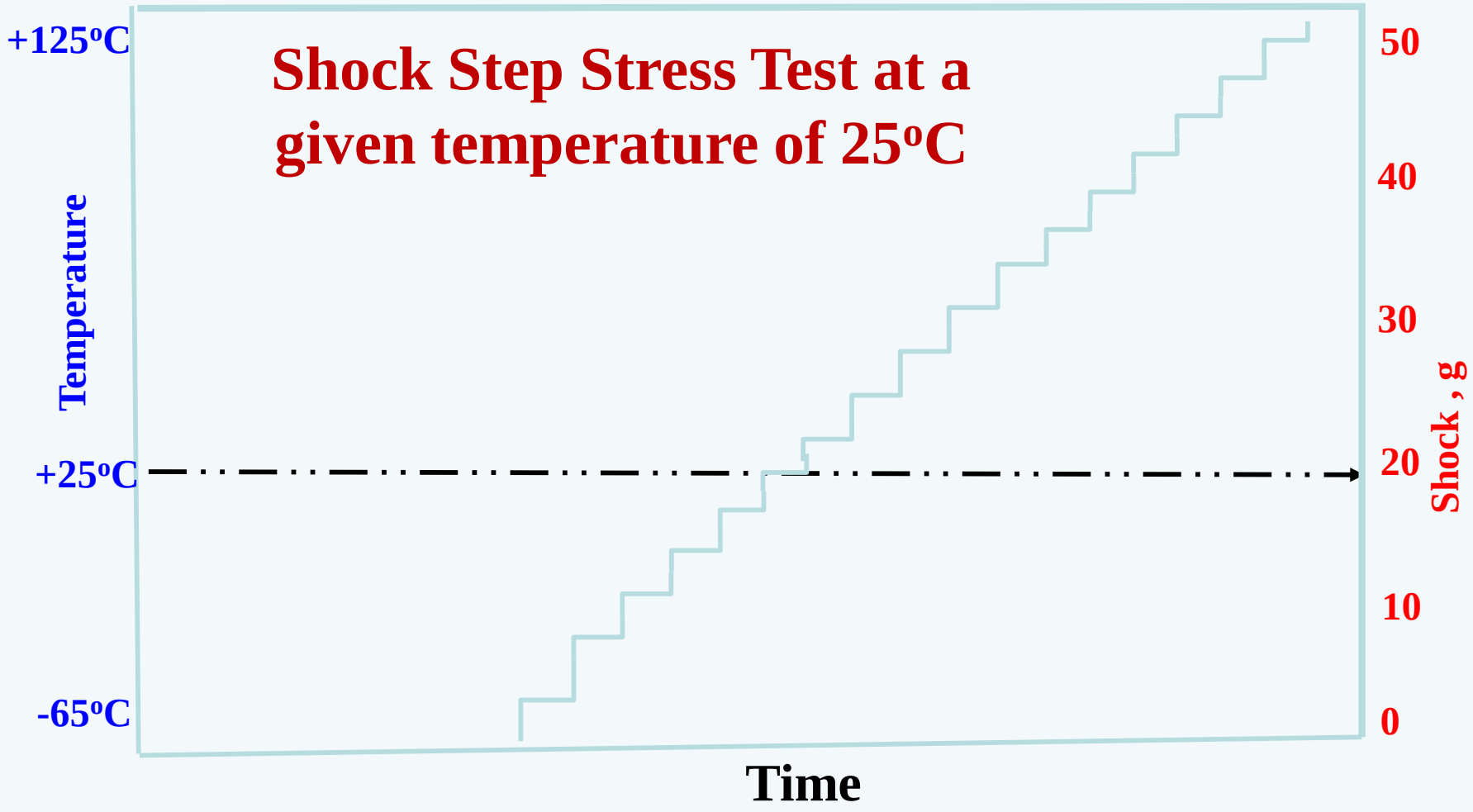


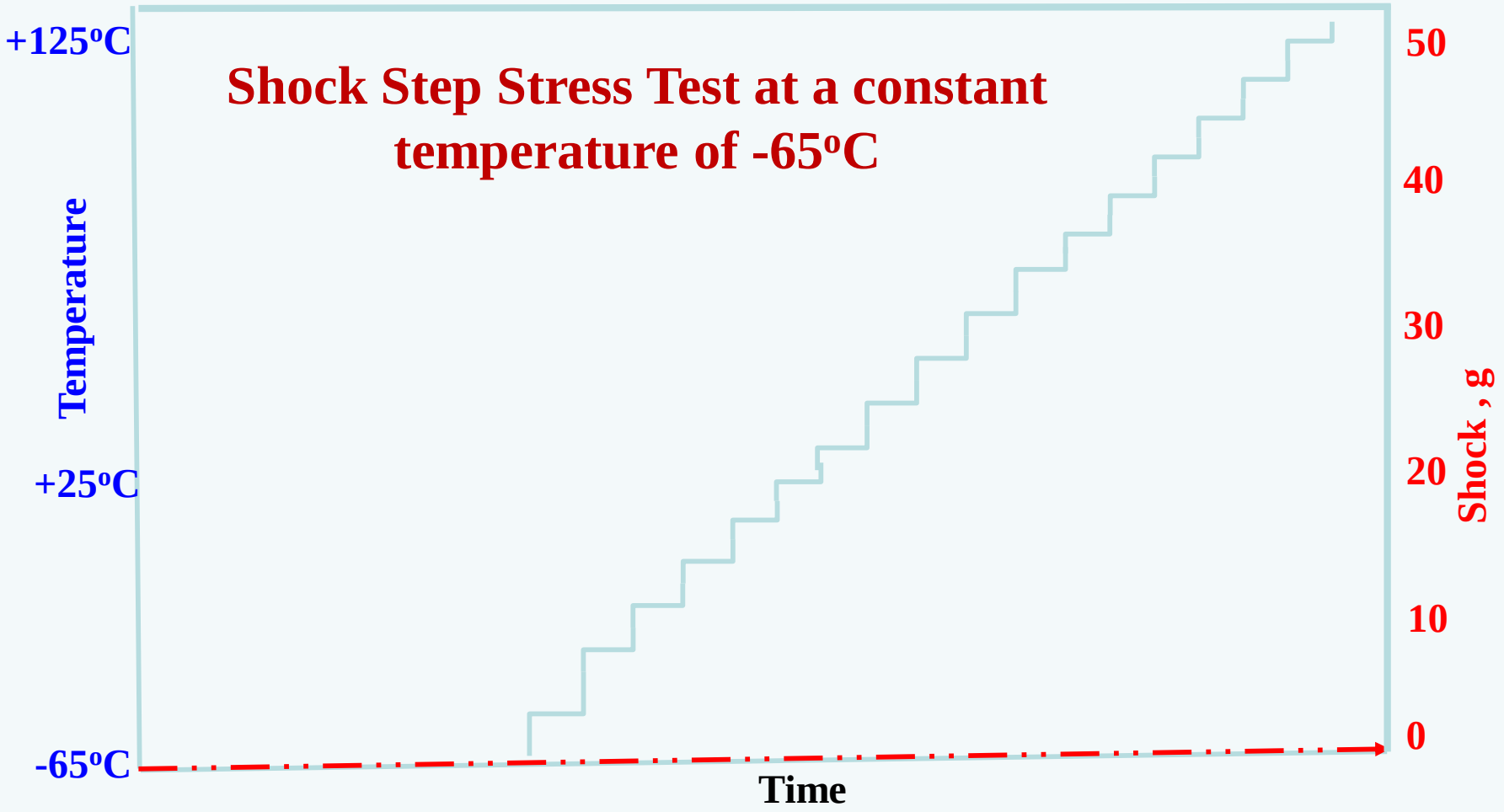
- Installed daisy-chained PBGA test boards in a HALT test chamber. HALT chamber has a thermal control (-55°C to +125°C) and mechanical shock control up to 50g. Initial tests have already been begun.
- Data logging system has been completed and tested to monitor the resistance of daisy chained PBGA packages during HALT test.
- The tests will be conducted in a temperature range of -65°C to +125°C. Developing a DoE to implement with the HALT with the above set-up.

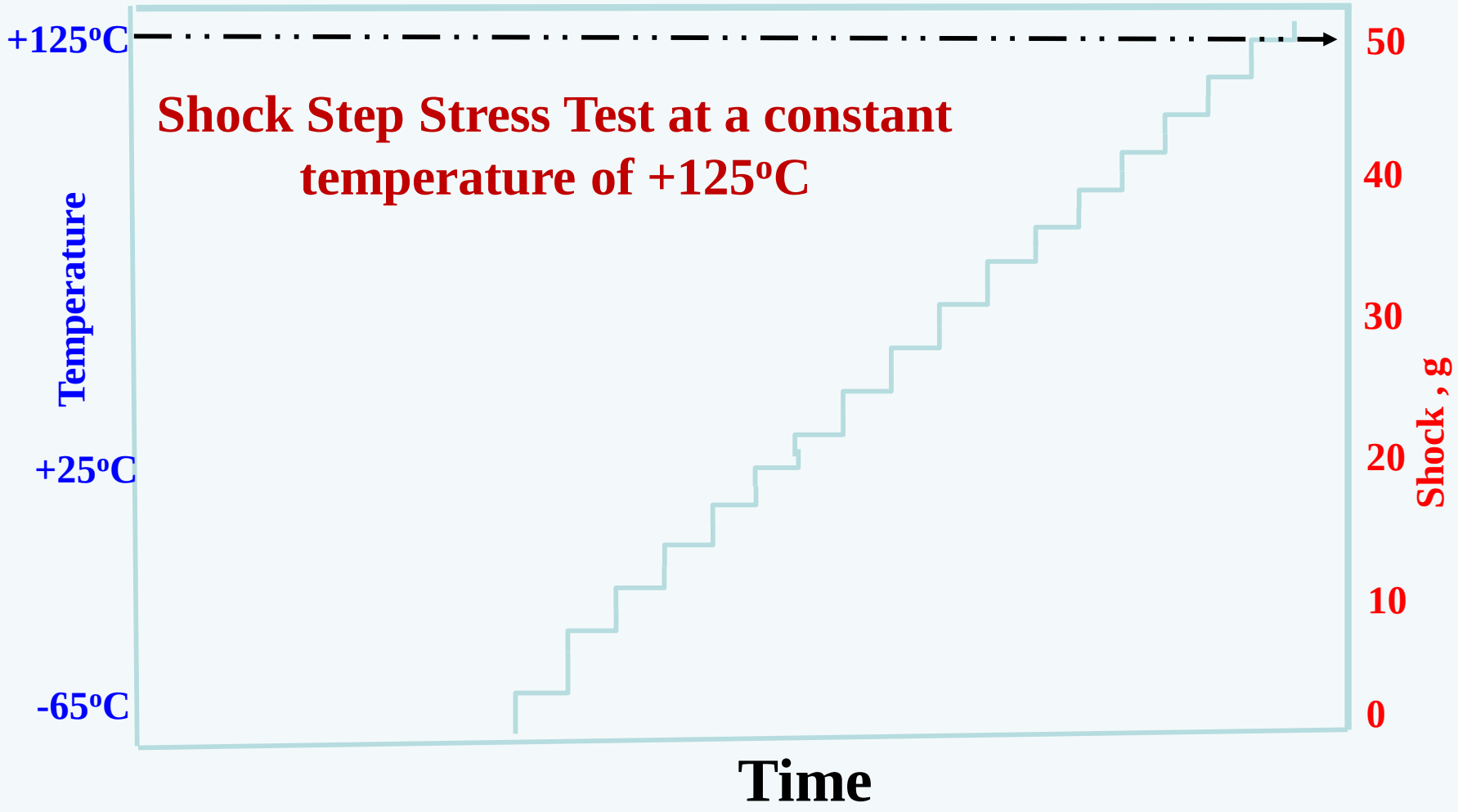

+125ºC
Temperature Step Stress Test
+25ºC to -65ºC to +125ºC at a
Certain temperature ramp rate
Temperature
+25ºC
-65ºC
Time

Rapid Thermal Transitions Stress Test

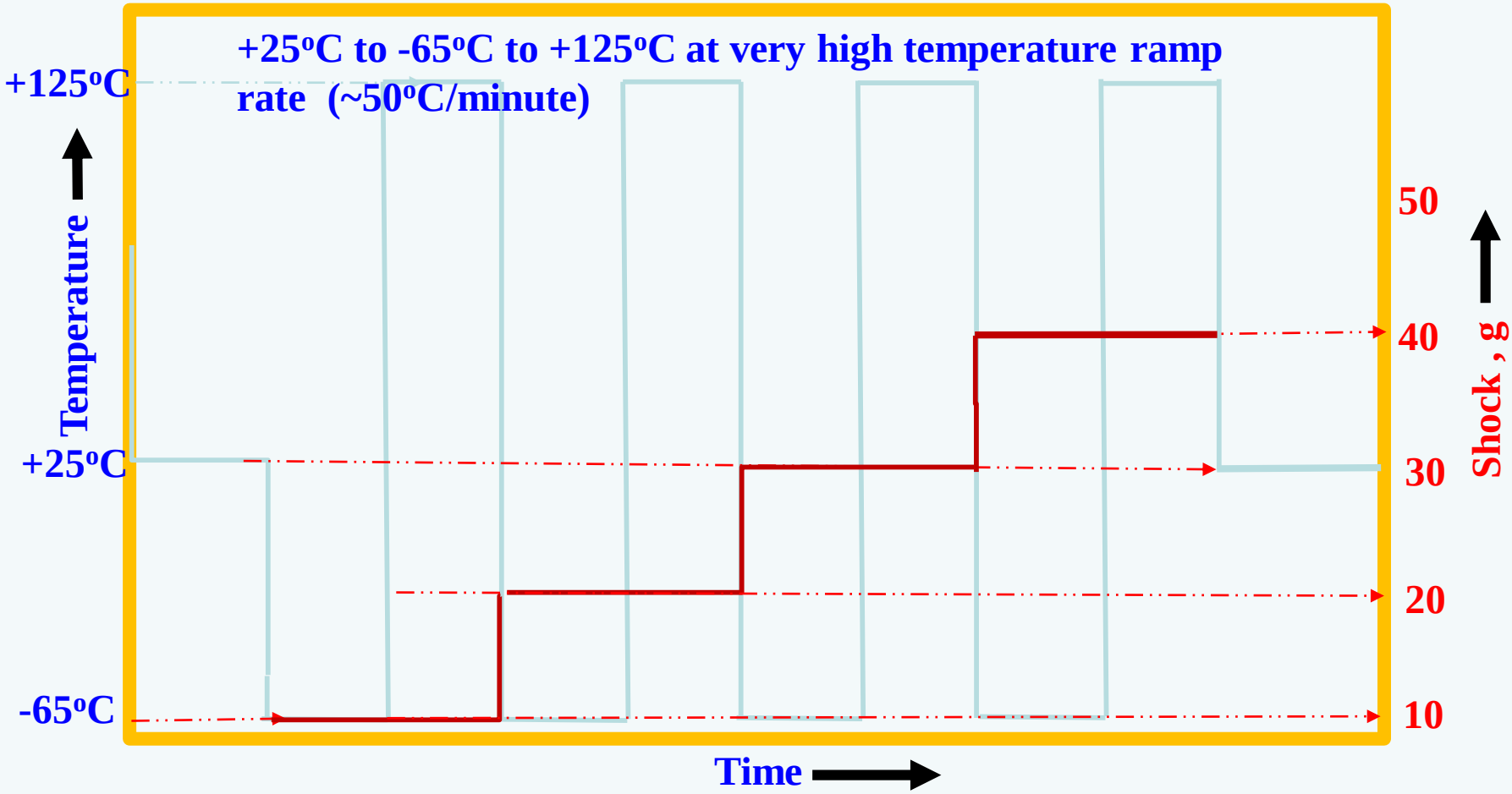



Shock Step Stress Test at a given temperature of 25ºC
+125ºC
+25ºC
-65ºC
Temperature
Time
50
40
30
20
10
0
Shock , g


Shock Step Stress Test at a constant temperature of -65ºC
+125ºC
+25ºC
-65ºC
Temperature
Time
50
40
30
20
10
0
Shock , g

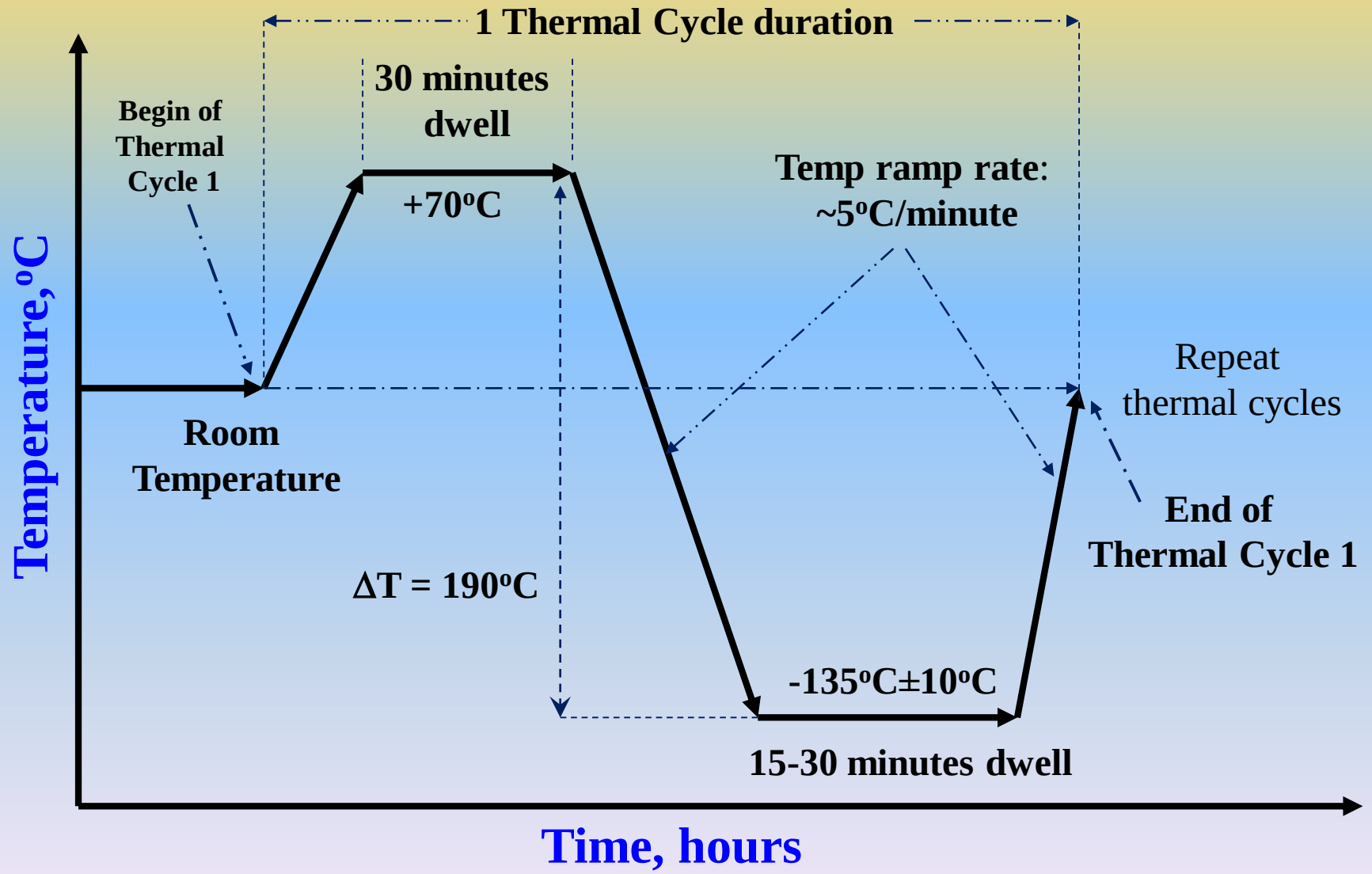

+125ºC
+25ºC
-65ºC
Temperature
Shock Step Stress Test at a constant temperature of +125ºC
50
40
30
20
10
0
Shock , g
Time

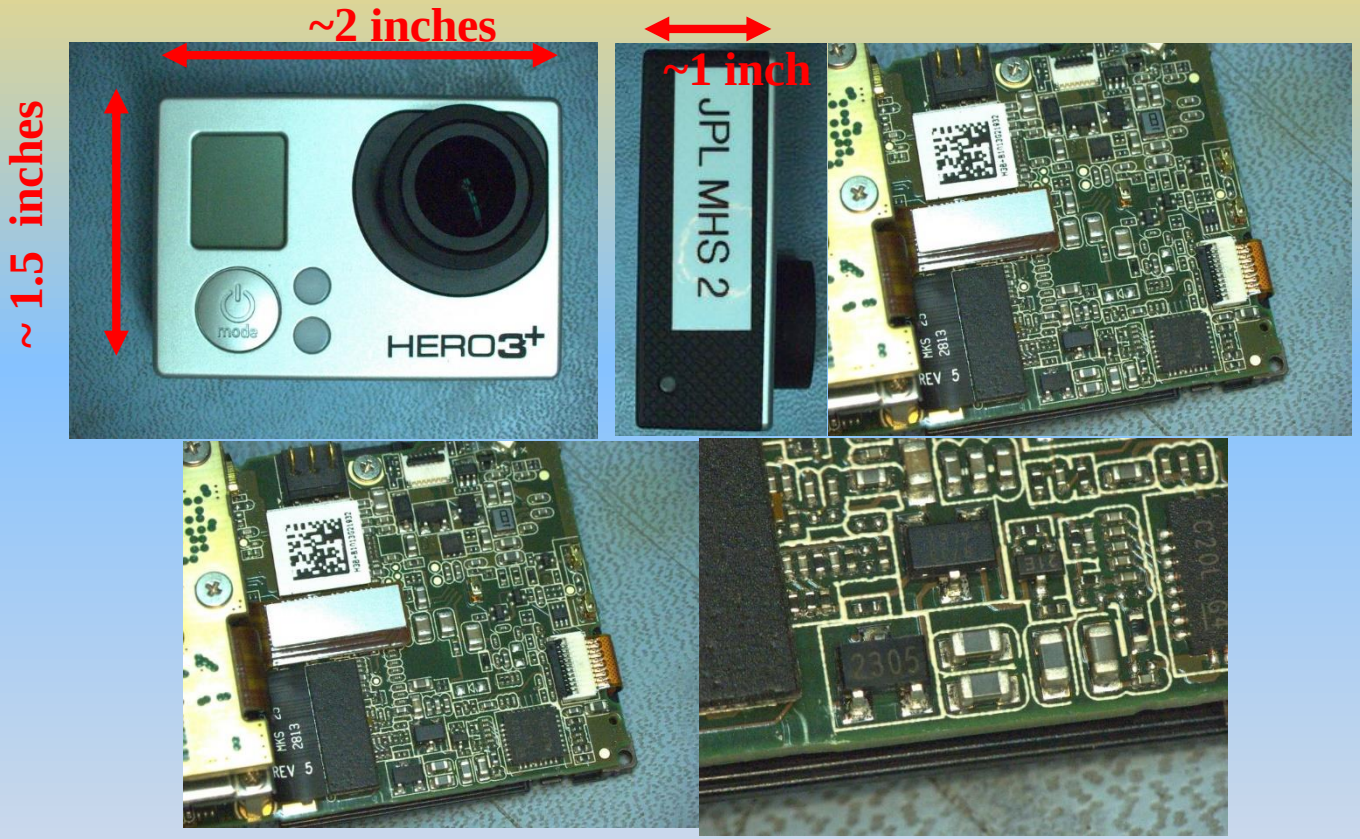
Combined Rapid Thermal Transitions Stress and Shock Test



GoPro Camera Thermal Cycling

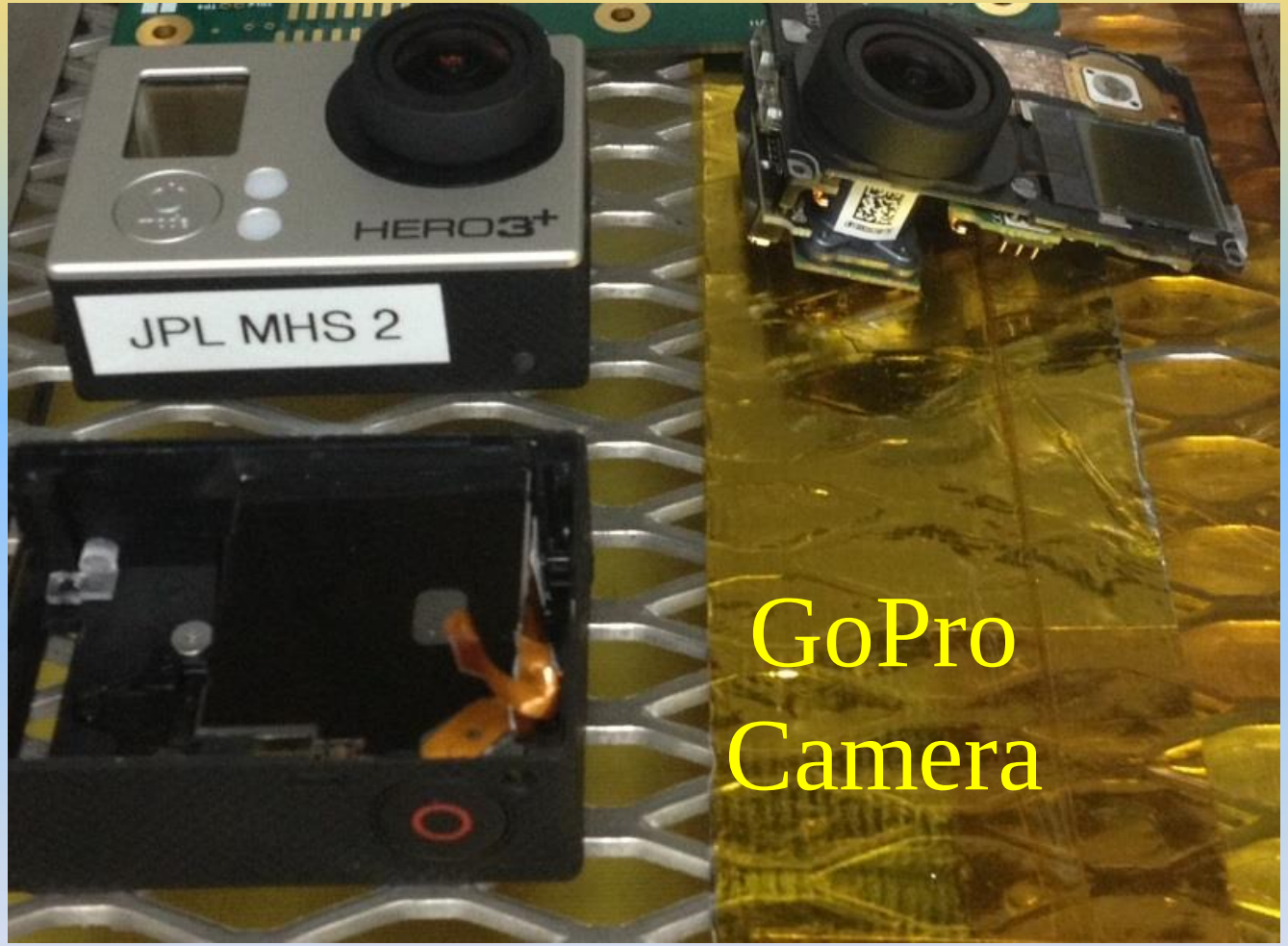
GoPro Camera Thermal Cycling





Miniaturized Passive Components

Passive Components in GoPro Camera for Mars Helicopter Applications



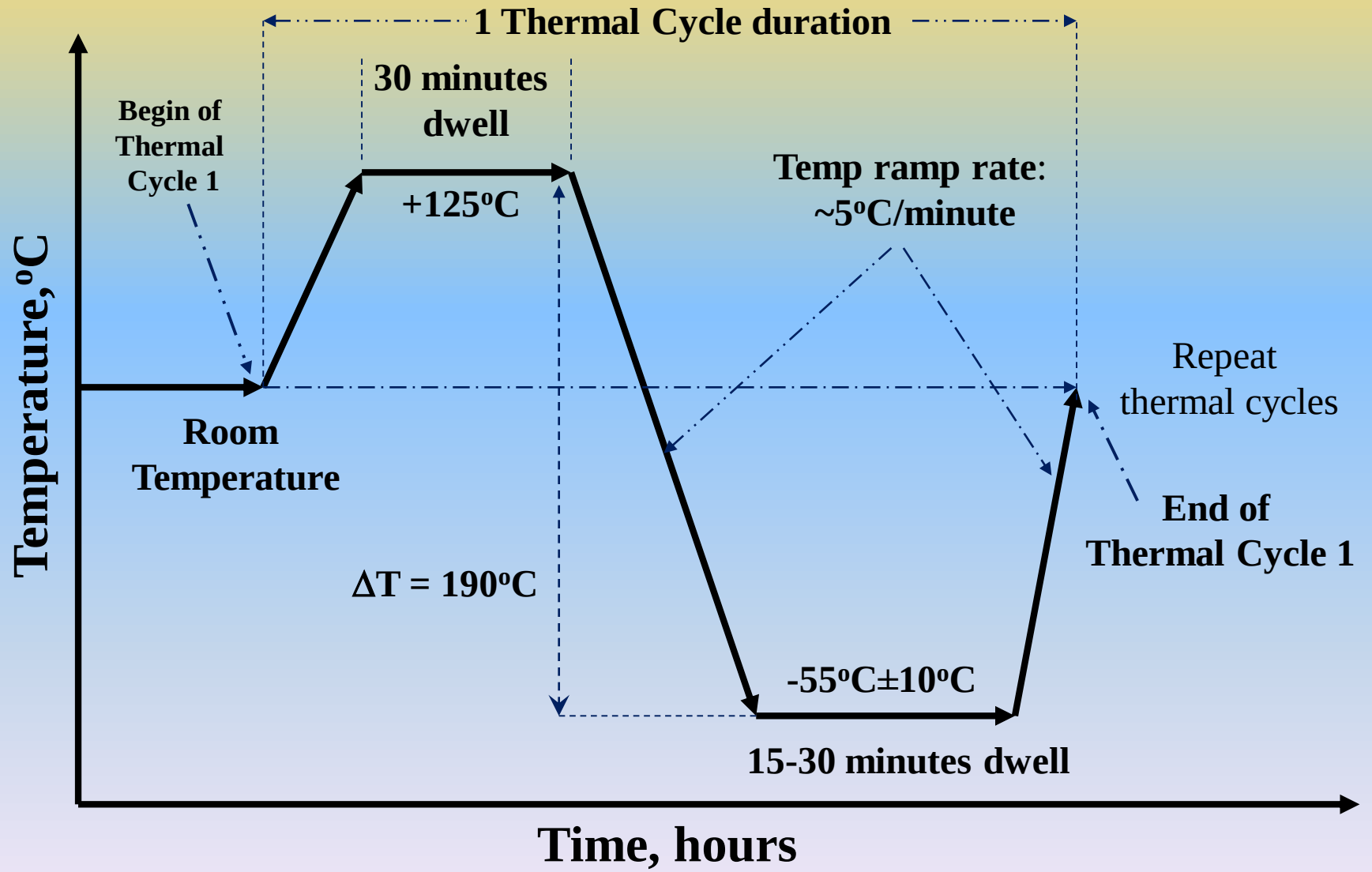
Passive Components in GoPro Camera for Mars Helicopter Applications

Thermal Cycling of GoPro Camera

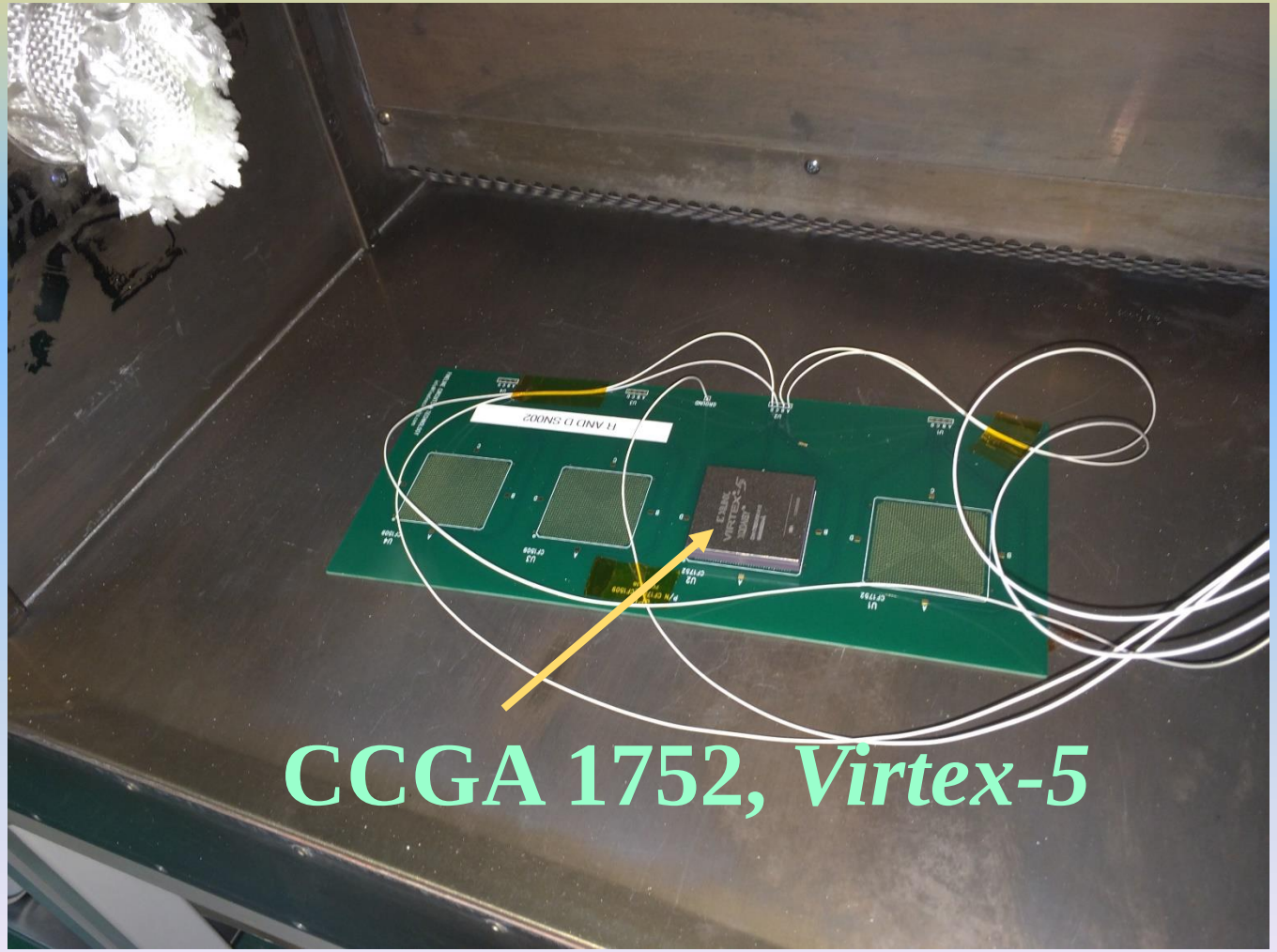
- **We completed a total of 193 thermal cycles from -135°C to +70°C.**
  - Camera is functional after thermal cycling
  - Battery was removed from the camera during thermal cycling.
  - Wireless communication has shown an anomaly after thermal cycling.
  - Further assessment plan are in progress to determine any problems with the electronic packaging.

CCGA 1752, *Virtex-5* Daisy-Chain Board

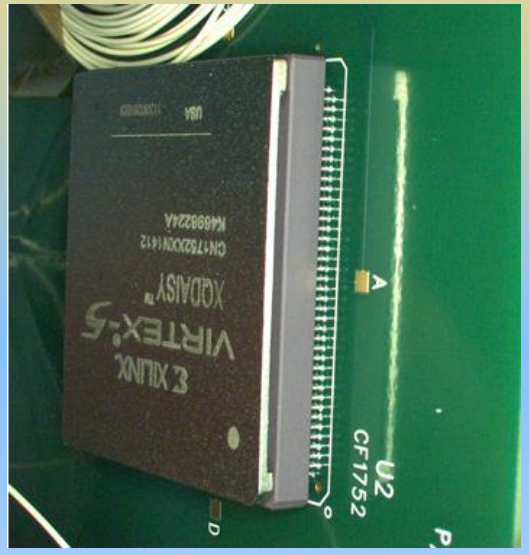
Thermal Cycling Profile (CCGA *Virtex-5*)

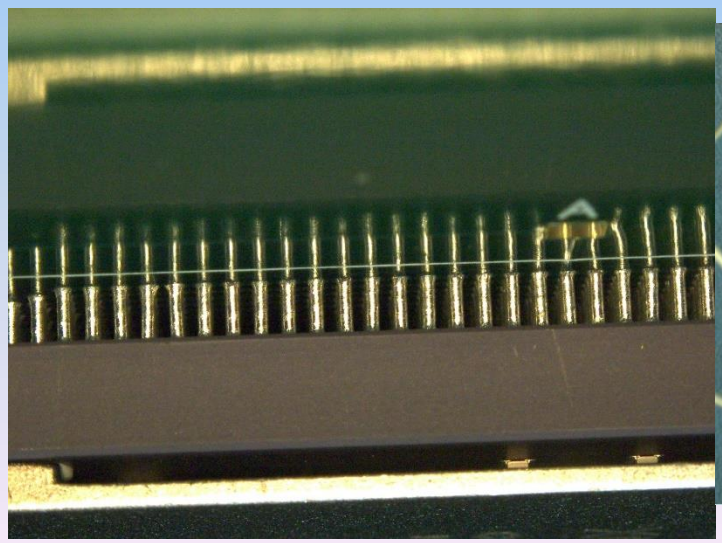


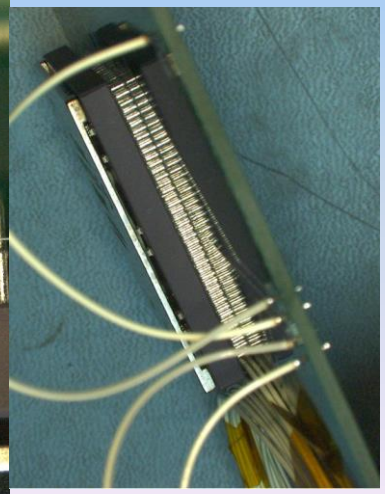
Assembled CCGA 1752 Advanced Kyocera Package

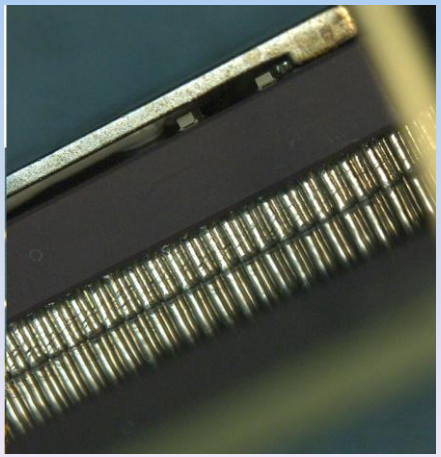


Assembled CCGA 1752 Advanced Kyocera Package

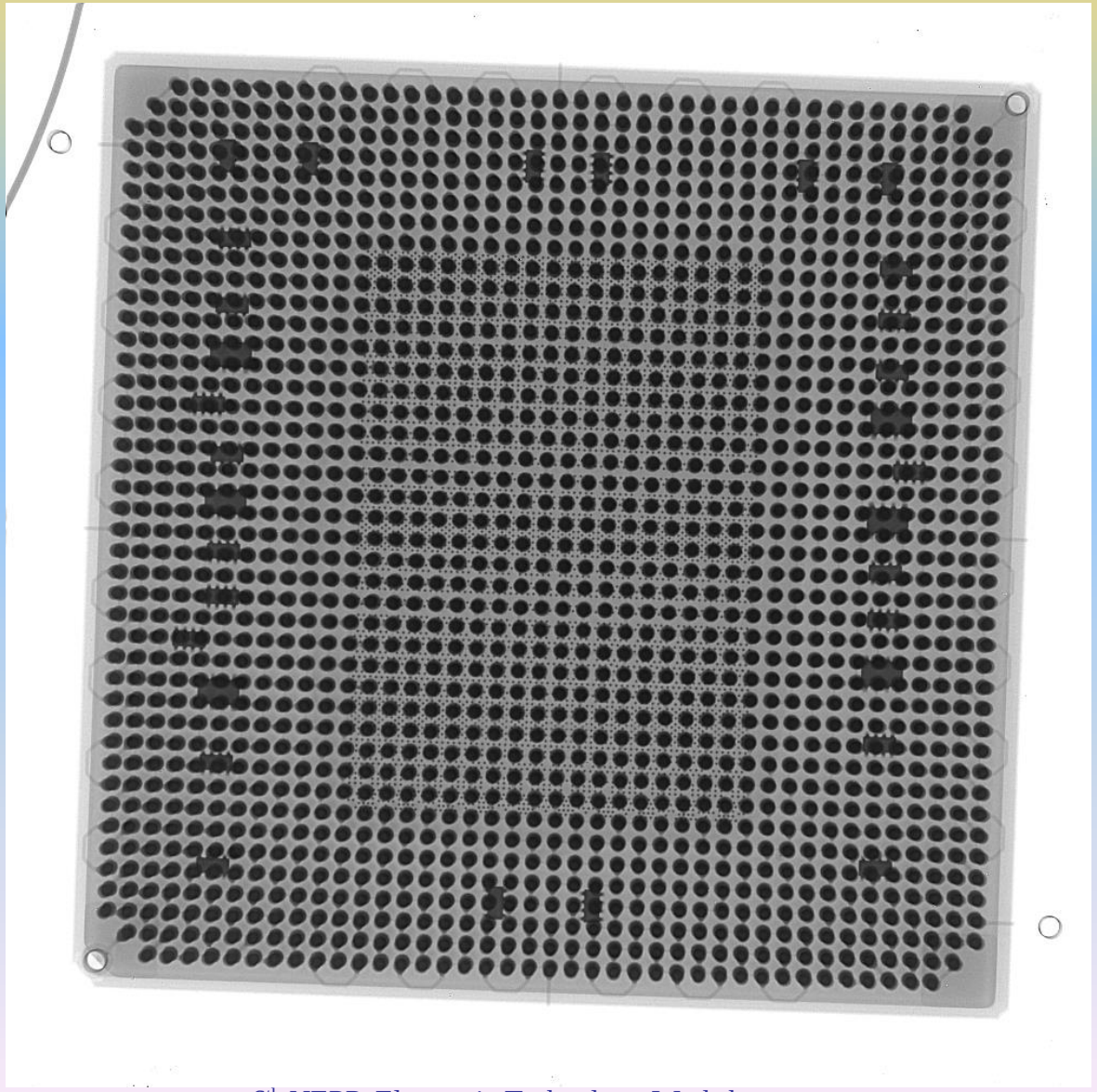




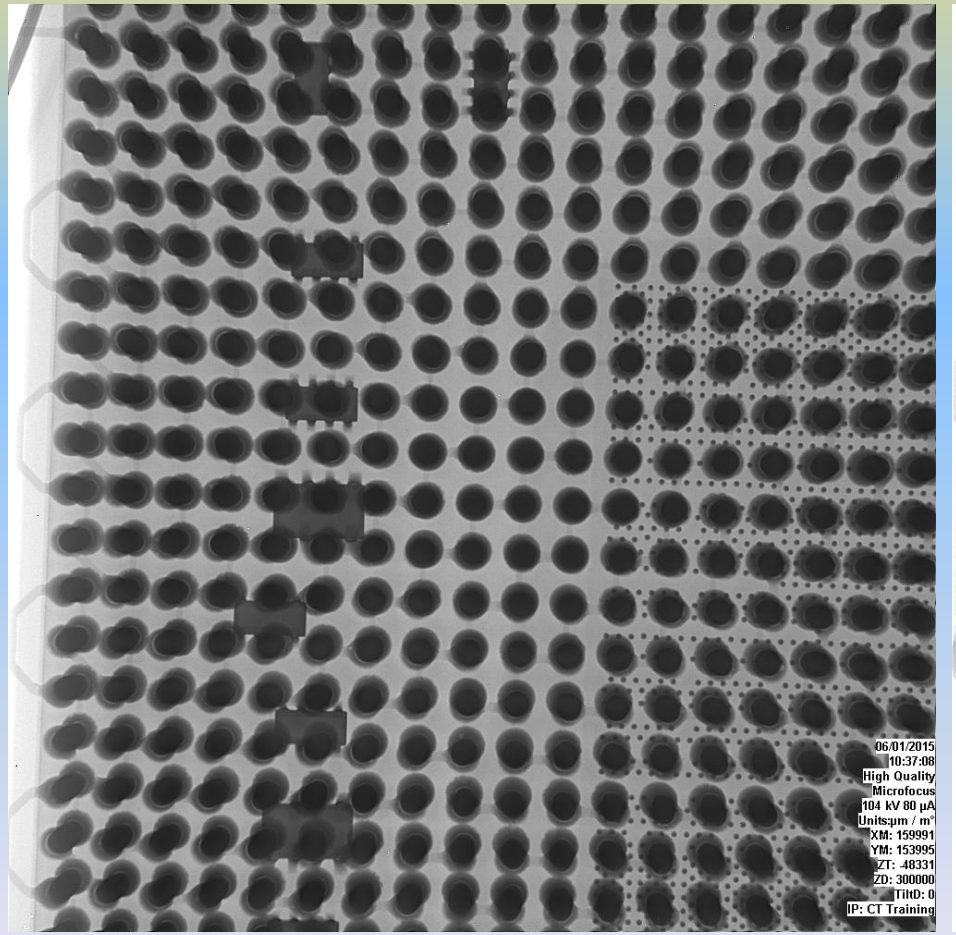


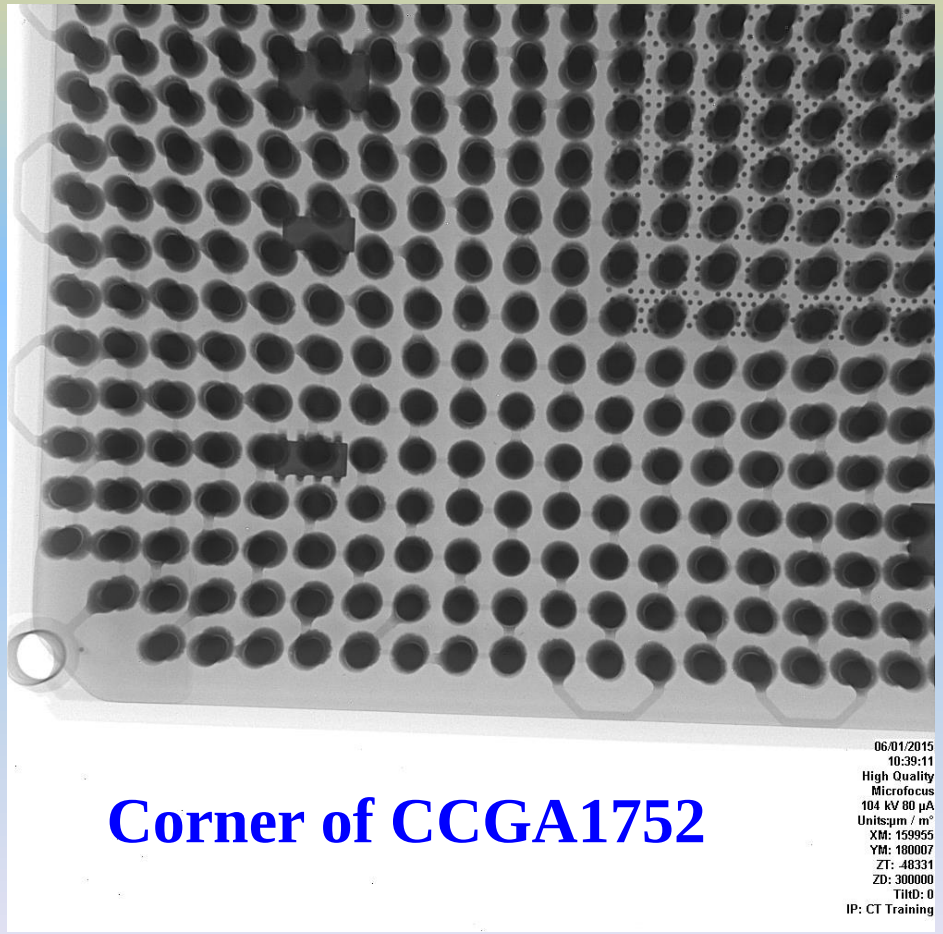


X-Ray Image of the assembled CCGA 1752 Advanced Kyocera Package

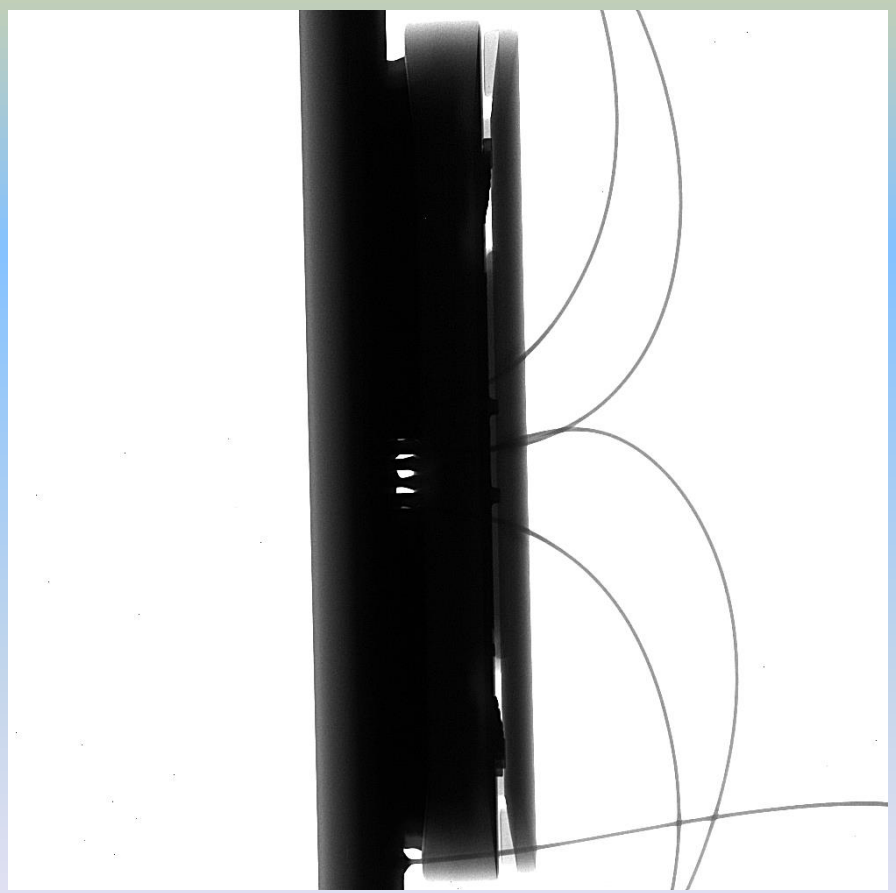


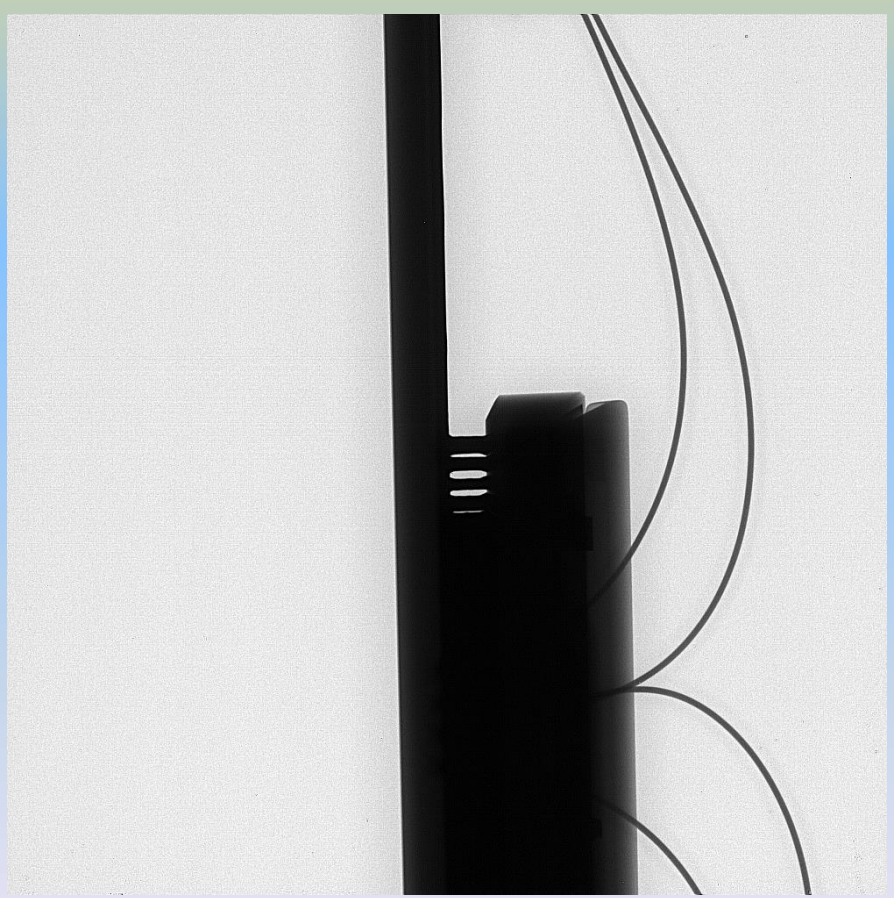
X-Ray Image of the assembled CCGA 1752 Advanced Kyocera Package



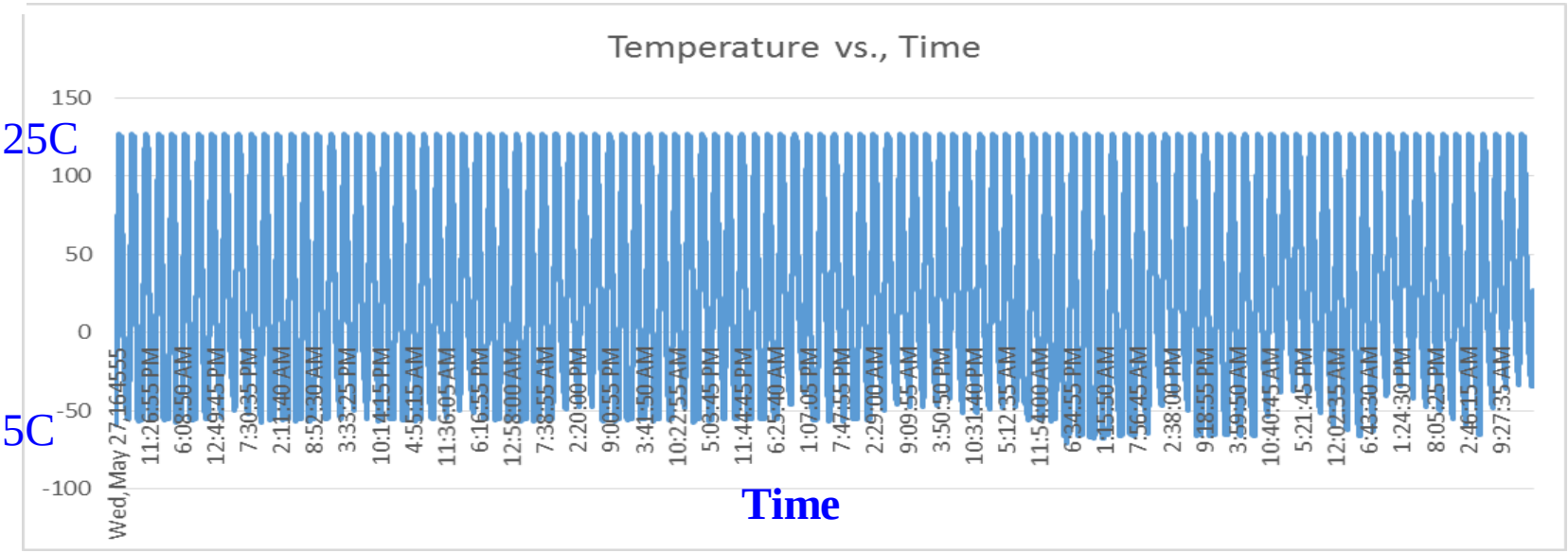


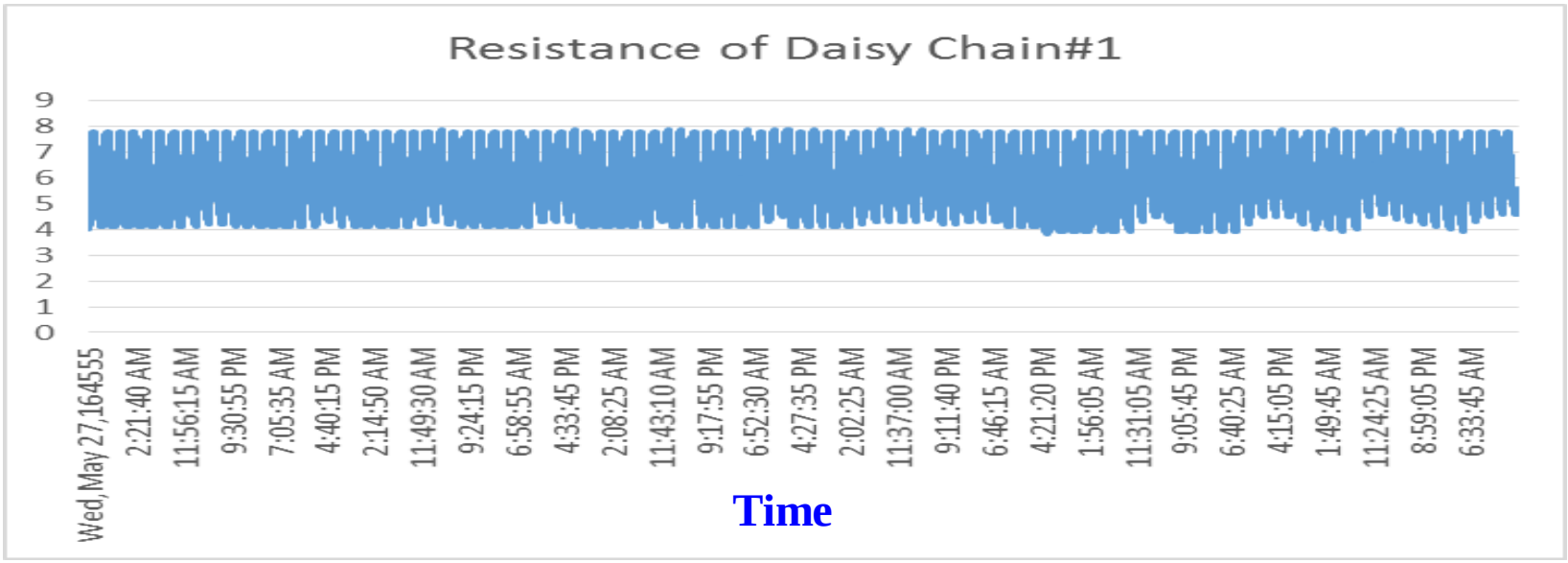
X-Ray Image of the assembled CCGA 1752 Advanced Kyocera Package at the Corner



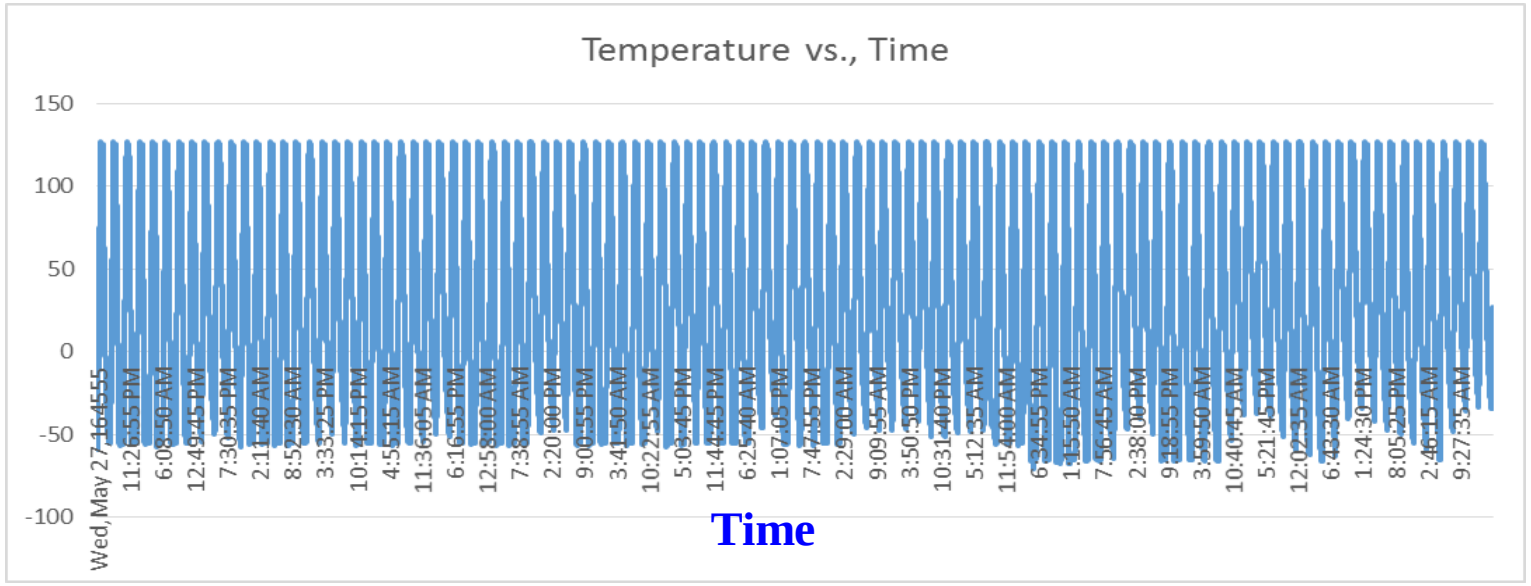


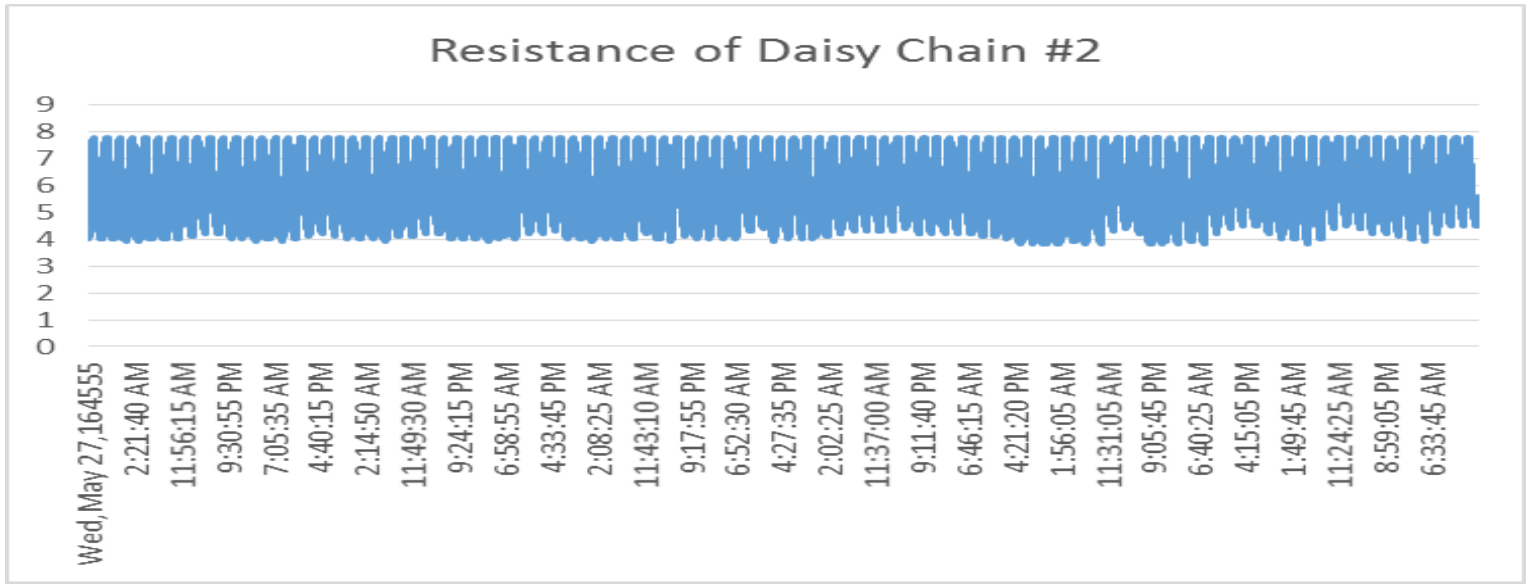
No anomalies like shorts were noted. Reflow quality of the columns and solder joints was good.



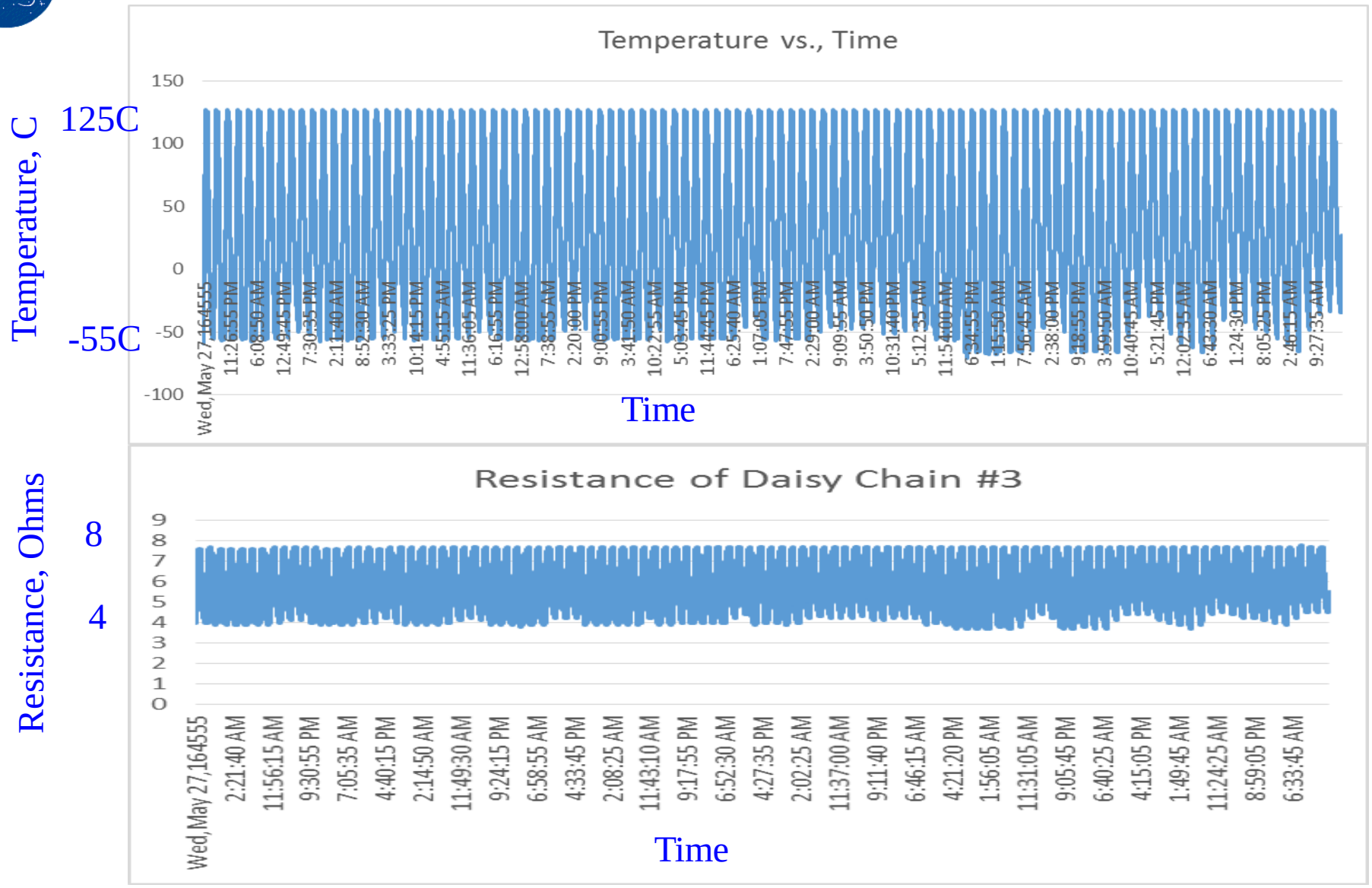


No change in daisy-chain resistance was observed which indicates no anomalies/failures.

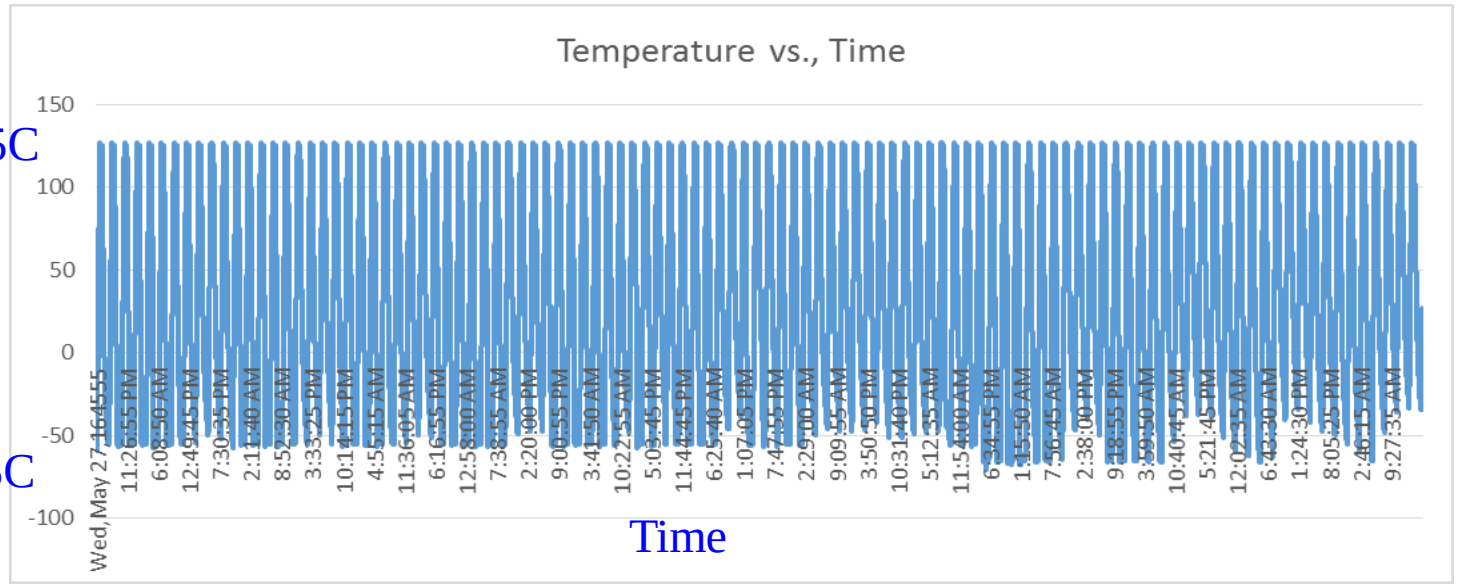


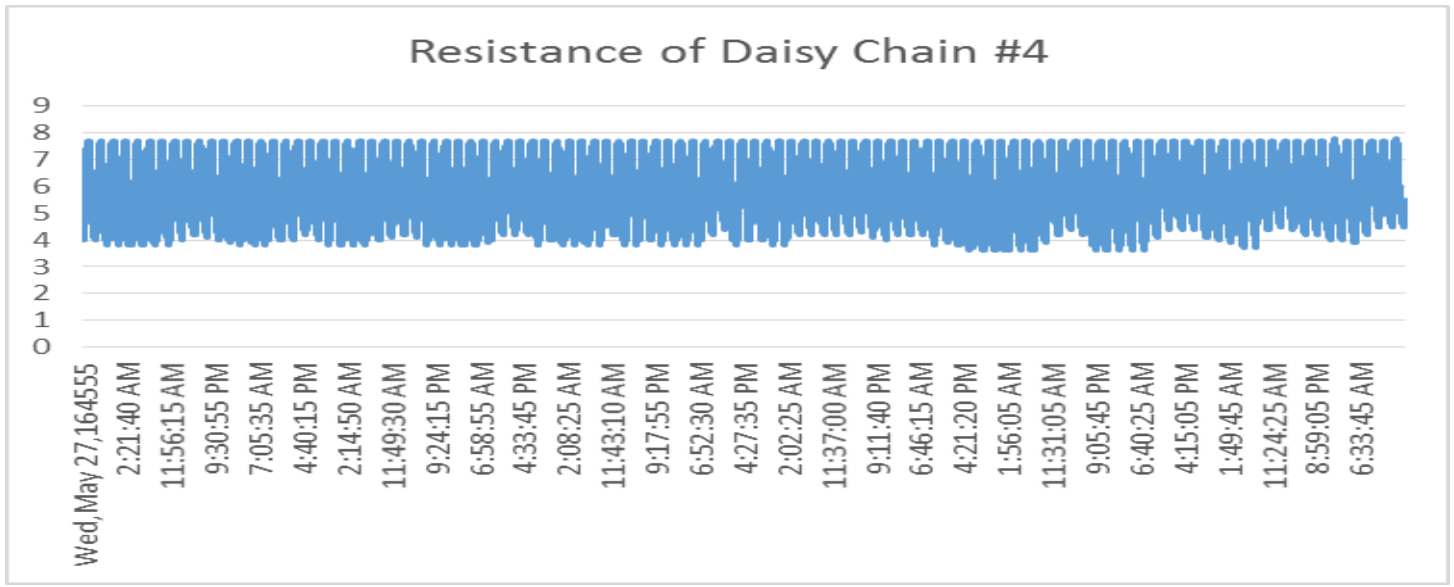


No change in daisy-chain resistance observed which indicates no anomalies/failures.



No change in daisy-chain resistance observed which indicates no anomalies/failures.





No change in daisy-chain resistance observed which indicates no anomalies/failures.

Summary-1

- Using of HALT technique to assess fatigue reliability of electronic packaging designs:
  - ✓ temperature range: –65°C to +125°C
  - ✓ acceleration range of up to 50g.
- The test boards were subjected to various g levels, dwell durations, and the hot and cold temperature levels. Advanced electronic packages have shown signs of continuity problems.
  - ✓ plastic ball grid array (PBGA)

  Designed a test board with various PBGA size packages and implementation of HALT technique to assess is in progress.
- *Virtex-5* CCGA board has been designed and fabricated. Base line thermal cycling data from -55°C±10 to +125°C.
  - – X-ray imaging of assembled CCGA 1752 is normal without any defects or anomalies.
  - – CCGA 1752 daisy-chain test boards with 250 thermal cycles. No anomalies were noted in daisy-chain resistance data.

Summary-2

- LCD display on *Xilinx V-5* board has started going bad after +75°C. The board went to dark (all the LEDs are not glowing) at +125°C. The LEDs have comeback once the temperature is below 75°C. Lost some segments though after high temperature exposure. LCD displays are sensitive to temperature above +75°C and cold temperatures down to -65°C.
- 12 Thermal cycles were performed from -65°C to +125°C. LCDs became completely black/not functional.
- Microsemi ASIC3/E board showed no problems even @ +125°C and also down to -65°C.
- Multi-Port Memory Controller (MPMC) Memory Test or External Memory Test failed in Spartan SP601 evaluation board at +125°C.
- Designed and fabricated cold and hot fixture for the shaker table. Preliminary assessment of the boards using HASS technique will be performed during the next few quarters.

Acknowledgements

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- Thanks are due to
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